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PLA00 LA6951P Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point

AIO M/B

2010-11-04

REV:0.3

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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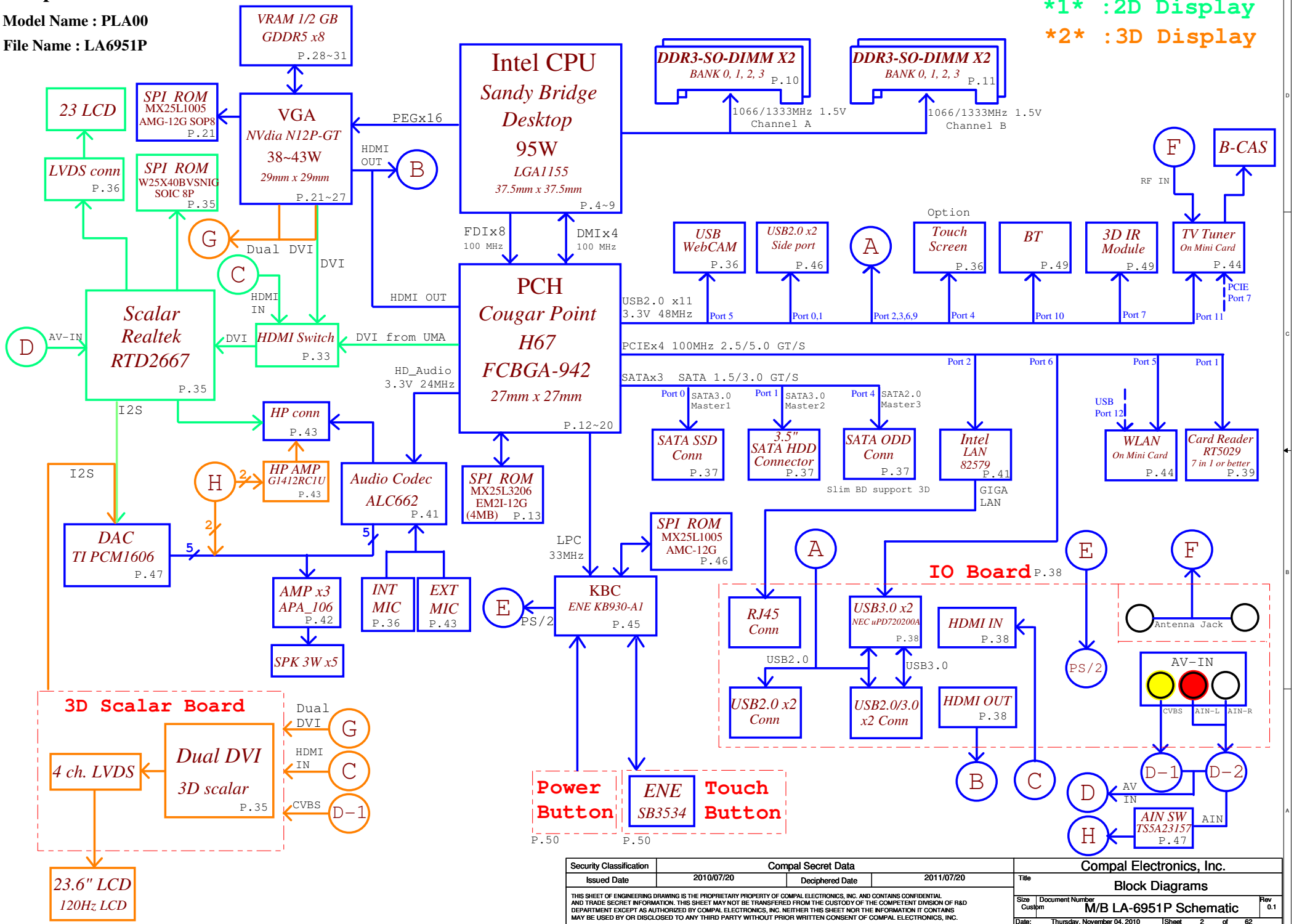
Model Name : PLA00

File Name : LA6951P

1 :2D Display

2 :3D Display



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Title: Block Diagrams

Size: Custom | Document Number: M/B LA-6951P Schematic | Rev: 0.1

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Voltage Rails

Power Plane	Description	S1	S3	S5
+12V1	Adapter power supply (12V)(For V_5V;V_3.3V;1.5V;12VS)	N/A	N/A	N/A
+12V2	Adapter power supply (12V)(For VGA_CORE;1.05VS;VRAM_1.5VS;CPU_CORE;VGFX_COREP)	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Graphics voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	1.05V switched power rail for PCH	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail once PS_ON# low	ON	ON	OFF
+3VSB	3.3V power rail befor PS_ON# low	ON	ON	ON
+3.3V_LAN	3.3V power rail for LAN	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+V_3.3V	3.3V power rail once Adapter plug-in	ON	ON	OFF
+V_5V	5V power rail once Adapter plug-in	ON	ON	OFF
+5VSB	5V power rail befor PS_ON# low	ON	ON	ON
+5VALW	5V always on power rail once PS_ON# low	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
+3VS_DGPU	3.3V power rail for GPU	ON	OFF	OFF
+VGA_CORE	Graphics power rail for GPU	ON	OFF	OFF
+1.05VS_DGPU	1.05VS switched power rail for GPU	ON	OFF	OFF
+VRAM_1.5VS	1.5VS power rail for VRAM	ON	OFF	OFF

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+VSB	+VS
Full ON	HIGH	HIGH	HIGH	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	OFF	ON	OFF

BOARD ID Table

Board ID	PCB Revision
* 0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID(Project) Table

Project_ID2 (GPIO38)	Project_ID1 (GPIO37)	Project_ID0 (GPIO36)	SKU
0	0	0	UMA@
0	0	1	DIS@(VRAM:Hynix)
0	1	0	DIS@(VRAM:Samsung)
0	1	1	X
1	0	0	X
1	0	1	X
1	1	0	X
1	1	1	X

EC SM Bus address

Device	Address
VGA Thermal Sensor(Internal)	0*9E H
VGA Thermal Sensor(External)	0*9A H

PCH SM Bus address

Device	Address
DDR(JDIMM1)	1010 0000 b
DDR(JDIMM2)	1010 0010 b
DDR(JDIMM4)	1010 0100 b
DDR(JDIMM3)	1010 0110 b

USB Port Table

USB 2.0	USB 1.1	Port	6 External USB Port
EHCI1	UHCI0	0	USB Conn.
		1	USB Conn
	UHCI1	2	USB Conn
		3	USB Conn
	UHCI2	4	Touch Screen
		5	Web Camera
	UHCI3	6	USB 2.0
		7	3D IR
EHCI2	UHCI4	8	
		9	USB 2.0
	UHCI5	10	Blue Tooth
		11	Mini Car(TV Tuner)
	UHCI6	12	Mini Car(WLAN)
		13	

BTO Option Table

BTO Item	BOM Structure
VGA	VGA@
UMA Only	UMA@
DIS Only	DIS@
2D	2D@
3D	3D@
VGA_2D	VGA_2D@
TAS3208	3208@
PCM1606	1606@
Samsung VRAM	X76_SAM@
Hynix VRAM	X76_HYN@
CRT	CRT@

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Title: Notes List

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DMI_PTX_HRX_N[0..3] <14>
DMI_PTX_HRX_P[0..3] <14>
DMI_HTX_PRX_N[0..3] <14>
DMI_HTX_PRX_P[0..3] <14>

PEG_GTX_C_HRX_P[0..15] <22>
PEG_GTX_C_HRX_N[0..15] <22>
PEG_HTX_C_GRX_P[0..15] <22>
PEG_HTX_C_GRX_N[0..15] <22>

JCPU1C SKT_H2

<REV>

Note:Use 0.1uF now; If need to support to Gen3, need change C1~C32 to 0.22uF.

PEG

PEG_GTX_C_HRX_P15	B11	PEG_RX[0]	PEG_TX[0]	C13	PEG_HTX_GRX_P15	C1	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_P15
PEG_GTX_C_HRX_N15	B12	PEG_RX#[0]	PEG_TX#[0]	C14	PEG_HTX_GRX_N15	C2	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_N15
PEG_GTX_C_HRX_P14	D12	PEG_RX[1]	PEG_TX[1]	E14	PEG_HTX_GRX_P14	C3	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_P14
PEG_GTX_C_HRX_N14	D11	PEG_RX#[1]	PEG_TX#[1]	E13	PEG_HTX_GRX_N14	C4	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_N14
PEG_GTX_C_HRX_P13	C10	PEG_RX[2]	PEG_TX[2]	G14	PEG_HTX_GRX_P13	C5	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_P13
PEG_GTX_C_HRX_N13	C9	PEG_RX#[2]	PEG_TX#[2]	G13	PEG_HTX_GRX_N13	C6	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_N13
PEG_GTX_C_HRX_P12	E10	PEG_RX[3]	PEG_TX[3]	F12	PEG_HTX_GRX_P12	C7	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_P12
PEG_GTX_C_HRX_N12	E9	PEG_RX#[3]	PEG_TX#[3]	F11	PEG_HTX_GRX_N12	C8	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_N12
PEG_GTX_C_HRX_P11	B8	PEG_RX[4]	PEG_TX[4]	J14	PEG_HTX_GRX_P11	C9	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_P11
PEG_GTX_C_HRX_N11	B7	PEG_RX#[4]	PEG_TX#[4]	J13	PEG_HTX_GRX_N11	C10	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_N11
PEG_GTX_C_HRX_P10	C6	PEG_RX[5]	PEG_TX[5]	D8	PEG_HTX_GRX_P10	C11	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_P10
PEG_GTX_C_HRX_N10	C5	PEG_RX#[5]	PEG_TX#[5]	D7	PEG_HTX_GRX_N10	C12	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_N10
PEG_GTX_C_HRX_P9	A5	PEG_RX[6]	PEG_TX[6]	D3	PEG_HTX_GRX_P9	C13	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_P9
PEG_GTX_C_HRX_N9	A6	PEG_RX#[6]	PEG_TX#[6]	C3	PEG_HTX_GRX_N9	C14	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_N9
PEG_GTX_C_HRX_P8	E2	PEG_RX[7]	PEG_TX[7]	E6	PEG_HTX_GRX_P8	C15	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_P8
PEG_GTX_C_HRX_N8	E1	PEG_RX#[7]	PEG_TX#[7]	E5	PEG_HTX_GRX_N8	C16	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_N8
PEG_GTX_C_HRX_P7	F4	PEG_RX[8]	PEG_TX[8]	F8	PEG_HTX_GRX_P7	C17	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_P7
PEG_GTX_C_HRX_N7	F3	PEG_RX#[8]	PEG_TX#[8]	F7	PEG_HTX_GRX_N7	C18	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_N7
PEG_GTX_C_HRX_P6	G2	PEG_RX[9]	PEG_TX[9]	G10	PEG_HTX_GRX_P6	C19	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_P6
PEG_GTX_C_HRX_N6	G1	PEG_RX#[9]	PEG_TX#[9]	G9	PEG_HTX_GRX_N6	C20	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_N6
PEG_GTX_C_HRX_P5	H3	PEG_RX[10]	PEG_TX[10]	G5	PEG_HTX_GRX_P5	C21	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_P5
PEG_GTX_C_HRX_N5	H4	PEG_RX#[10]	PEG_TX#[10]	G6	PEG_HTX_GRX_N5	C22	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_N5
PEG_GTX_C_HRX_P4	J1	PEG_RX[11]	PEG_TX[11]	K7	PEG_HTX_GRX_P4	C23	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_P4
PEG_GTX_C_HRX_N4	J2	PEG_RX#[11]	PEG_TX#[11]	K8	PEG_HTX_GRX_N4	C24	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_N4
PEG_GTX_C_HRX_P3	K3	PEG_RX[12]	PEG_TX[12]	J5	PEG_HTX_GRX_P3	C25	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_P3
PEG_GTX_C_HRX_N3	K4	PEG_RX#[12]	PEG_TX#[12]	J6	PEG_HTX_GRX_N3	C26	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_N3
PEG_GTX_C_HRX_P2	L1	PEG_RX[13]	PEG_TX[13]	M8	PEG_HTX_GRX_P2	C27	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_P2
PEG_GTX_C_HRX_N2	L2	PEG_RX#[13]	PEG_TX#[13]	M7	PEG_HTX_GRX_N2	C28	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_N2
PEG_GTX_C_HRX_P1	M3	PEG_RX[14]	PEG_TX[14]	L6	PEG_HTX_GRX_P1	C29	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_P1
PEG_GTX_C_HRX_N1	M4	PEG_RX#[14]	PEG_TX#[14]	L5	PEG_HTX_GRX_N1	C30	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_N1
PEG_GTX_C_HRX_P0	N1	PEG_RX[15]	PEG_TX[15]	N5	PEG_HTX_GRX_P0	C31	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_P0
PEG_GTX_C_HRX_N0	N2	PEG_RX#[15]	PEG_TX#[15]	N6	PEG_HTX_GRX_N0	C32	1	2	VGA@.1U_0402_16V7K	PEG_HTX_C_GRX_N0

DMI

DMI_PTX_HRX_P0	W5	DMI_RX[0]	DMI_TX[0]	V7	DMI_HTX_PRX_P0
DMI_PTX_HRX_N0	W4	DMI_RX#[0]	DMI_TX#[0]	V6	DMI_HTX_PRX_N0
DMI_PTX_HRX_P1	V3	DMI_RX[1]	DMI_TX[1]	W7	DMI_HTX_PRX_P1
DMI_PTX_HRX_N1	V4	DMI_RX#[1]	DMI_TX#[1]	W8	DMI_HTX_PRX_N1
DMI_PTX_HRX_P2	Y3	DMI_RX[2]	DMI_TX[2]	Y6	DMI_HTX_PRX_P2
DMI_PTX_HRX_N2	Y4	DMI_RX#[2]	DMI_TX#[2]	Y7	DMI_HTX_PRX_N2
DMI_PTX_HRX_P3	AA4	DMI_RX_3	DMI_TX[3]	AA7	DMI_HTX_PRX_P3
DMI_PTX_HRX_N3	AA5	DMI_RX#[3]	DMI_TX#[3]	AA8	DMI_HTX_PRX_N3

GEN

P3	PE_RX[0]	PE_TX[0]	P8
P4	PE_RX#[0]	PE_TX#[0]	P7
R2	PE_RX[1]	PE_TX[1]	T7
R1	PE_RX#[1]	PE_TX#[1]	T8
T4	PE_RX[2]	PE_TX[2]	R6
T3	PE_RX#[2]	PE_TX#[2]	R5
U2	PE_RX[3]	PE_TX[3]	U5
U1	PE_RX#[3]	PE_TX#[3]	U6

7/20 PE_RX[0~3]/PE_RX#[0~3] only use on Workstation.

7/20 PE_TX[0~3]/PE_TX#[0~3] only use on Workstation.

+1.05VS

24.9_0402_1% 2 1 R1 PEG_IRCOMP

B5	PEG_ICOMPO	
C4	PEG_RCOMPO	
B4	PEG_ICOMPI	

LOTES_ACAZIF096P01_SANDYBRIDGE 3 OF 11 CONN@

PEG_ICOMPI and RCOMPO signals should be shorted and routed
with - max length = 500 mils - ;Width/Space= (4 mils/15mils)
PEG_ICOMPO signals should be routed with - max length = 500 mils
- Width/Space (12 mils/15mils)

1000P_0402_50V7K @ 2 1 C1007 H_FDI_FSYNC0
1000P_0402_50V7K @ 2 1 C1008 H_FDI_LSYNC0
1000P_0402_50V7K @ 2 1 C1009 H_FDI_FSYNC1
1000P_0402_50V7K @ 2 1 C1010 H_FDI_LSYNC1
1000P_0402_50V7K @ 2 1 C1011 H_FDI_INT

8/23 Add

H_FDI_TXN[0..7] <16>
H_FDI_TXP[0..7] <16>

JCPU1D SKT_H2

FDI_TX[0]

<16> H_FDI_FSYNC0	AC5	FDI_FSYNC_0	FDI_TX[0]	AC8	H_FDI_TXP0
<16> H_FDI_LSYNC0	AC4	FDI_LSYNC_0	FDI_TX#[0]	AC7	H_FDI_TXN0
			FDI_TX[1]	AC2	H_FDI_TXP1
			FDI_TX#[1]	AC3	H_FDI_TXN1
			FDI_TX[2]	AD2	H_FDI_TXP2
			FDI_TX#[2]	AD1	H_FDI_TXN2
			FDI_TX[3]	AD4	H_FDI_TXP3
			FDI_TX#[3]	AD3	H_FDI_TXN3
			FDI_TX[4]	AD7	H_FDI_TXP4
			FDI_TX#[4]	AD6	H_FDI_TXN4
			FDI_TX[5]	AE7	H_FDI_TXP5
			FDI_TX#[5]	AE8	H_FDI_TXN5
			FDI_TX[6]	AF3	H_FDI_TXP6
			FDI_TX#[6]	AF2	H_FDI_TXN6
			FDI_TX[7]	AG2	H_FDI_TXP7
			FDI_TX#[7]	AG1	H_FDI_TXN7
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<16> H_FDI_LSYNC1	AE4	FDI_LSYNC_1			
<16> H_FDI_INT	AG3	FDI_INT			
+1.05VS		24.9_0402_1% 2 1 R2	FDI_ICOMP	AE2	FDI_COMPIO
				AE1	FDI_ICOMPO

FDI LINK

LOTES_ACAZIF096P01_SANDYBRIDGE 4 OF 11 CONN@

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Title: PROCESSOR (1/6) DMI,FDI,PEG

Size	Document Number	Rev
B	PLA00 M/B LA-6951P Schematic	0.3

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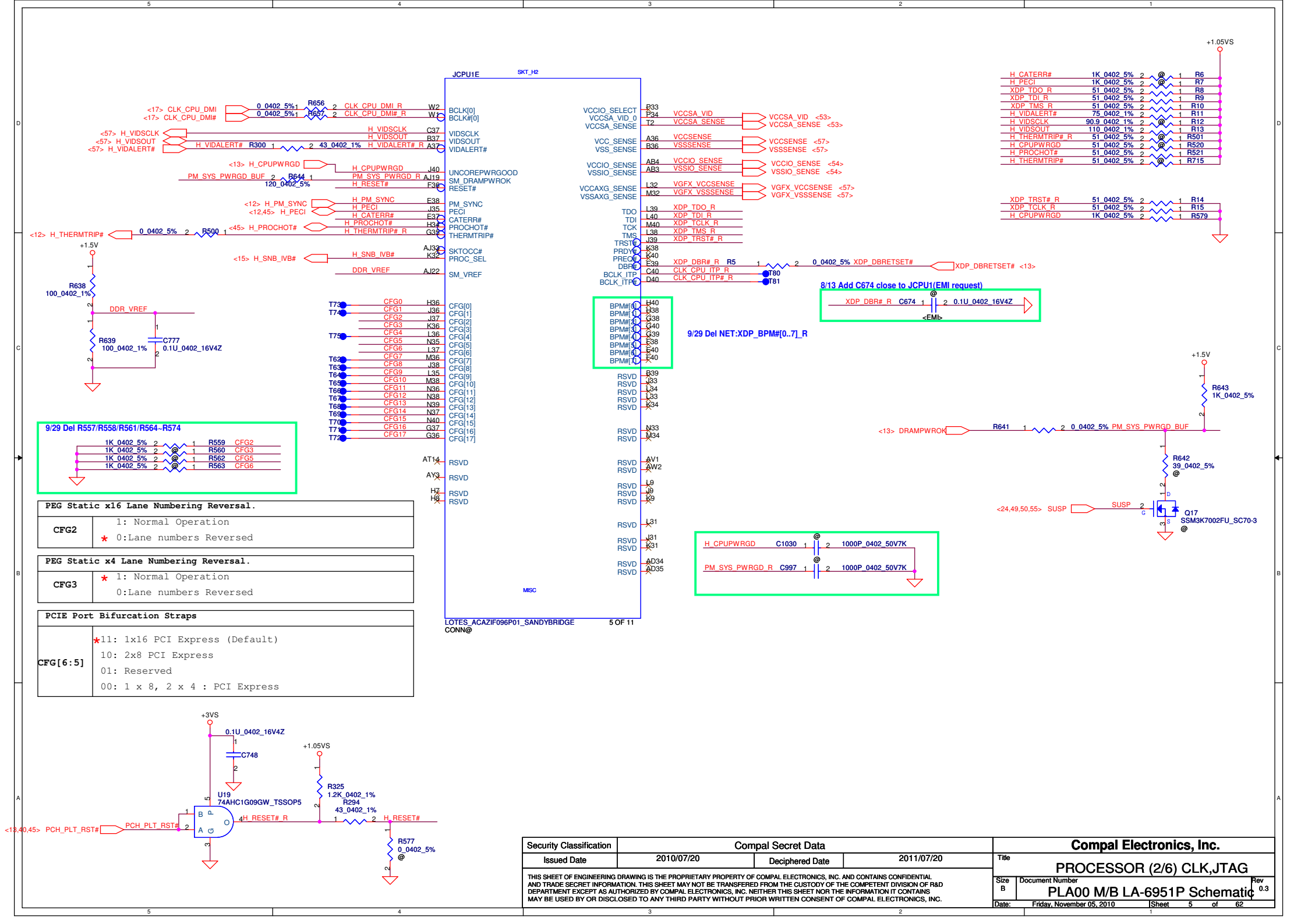
JCPU1E
SKT_H2
LOTES_ACAZIF096P01_SANDYBRIDGE
CONN@
5 OF 11
MISC
BCLK[0]
BCLK#[0]
VIDSCLK
VIDSOUT
VIDALERT#
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#
PM_SYNC
PECI
CATERR#
PROCHOT#
THERMTRIP#
SKTOCC#
PROC_SEL
SM_VREF
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VCCSA_SENSE
VCC_SENSE
VSS_SENSE
VCCIO_SENSE
VSSIO_SENSE
VCCAXG_SENSE
VSSAXG_SENSE
TDO
TDI
TCK
TMS
TRST#
PRDY#
PREQ#
DBR#
BCLK_ITP
BCLK_ITP#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
BPM#[4]
BPM#[5]
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BPM#[7]
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CLK_CPU_DMI#_R
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H_VIDALERT#_R
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H_CATERR#
<45> H_PROCHOT#
H_PROCHOT#_R
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H_SNB_IVB#
DDR_VREF
VCCSA_VID
VCCSA_SENSE
VCCSENSE
VSSSENSE
VCCIO_SENSE
VSSIO_SENSE
VGFX_VCCSENSE
VGFX_VSSSENSE
XDP_TDO_R
XDP_TDI_R
XDP_TCLK_R
XDP_TMS_R
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R656
R657
R300
R644
120_0402_5%
43_0402_1%
R500
R638
100_0402_1%
R639
100_0402_1%
C777
0.1U_0402_16V4Z
R5
0_0402_5%
T80
T81
T73
T74
T75
T62
T63
T64
T65
T66
T67
T68
T69
T70
T71
T72
+1.5V
+1.05VS
9/29 Del R557/R558/R561/R564~R574
1K_0402_5%
R559
R560
R562
R563
CFG2
CFG3
CFG5
CFG6
8/13 Add C674 close to JCPU1(EMI request)
C674
0.1U_0402_16V4Z
<EMI>
9/29 Del NET:XDP_BPM#[0..7]_R
H_CATERR#
H_PECI
XDP_TDO_R
XDP_TDI_R
XDP_TMS_R
H_VIDALERT#
H_VIDSCLK
H_VIDSOUT
H_THERMTRIP#_R
H_CPUPWRGD
H_PROCHOT#
H_THERMTRIP#
R6
R7
R8
R9
R10
R11
R12
R13
R501
R520
R521
R715
XDP_TRST#_R
XDP_TCLK_R
R14
R15
R579
R643
1K_0402_5%
<13> DRAMPWROK
R641
PM_SYS_PWRGD_BUF
R642
39_0402_5%
<24,49,50,55> SUSP
Q17
SSM3K7002FU_SC70-3
H_CPUPWRGD
C1030
PM_SYS_PWRGD_R
C997
1000P_0402_50V7K
PEG Static x16 Lane Numbering Reversal.
CFG2
1: Normal Operation
* 0:Lane numbers Reversed
PEG Static x4 Lane Numbering Reversal.
CFG3
* 1: Normal Operation
0:Lane numbers Reversed
PCIE Port Bifurcation Straps
CFG[6:5]
*11: 1x16 PCI Express (Default)
10: 2x8 PCI Express
01: Reserved
00: 1 x 8, 2 x 4 : PCI Express
+3VS
0.1U_0402_16V4Z
C748
U19
74AHC1G09GW_TSSOP5
R325
1.2K_0402_1%
R294
43_0402_1%
<13,40,45> PCH_PLT_RST#
PCH_PLT_RST#
H_RESET#_R
H_RESET#
R577
0_0402_5%
Security Classification
Compal Secret Data
Issued Date
2010/07/20
Deciphered Date
2011/07/20
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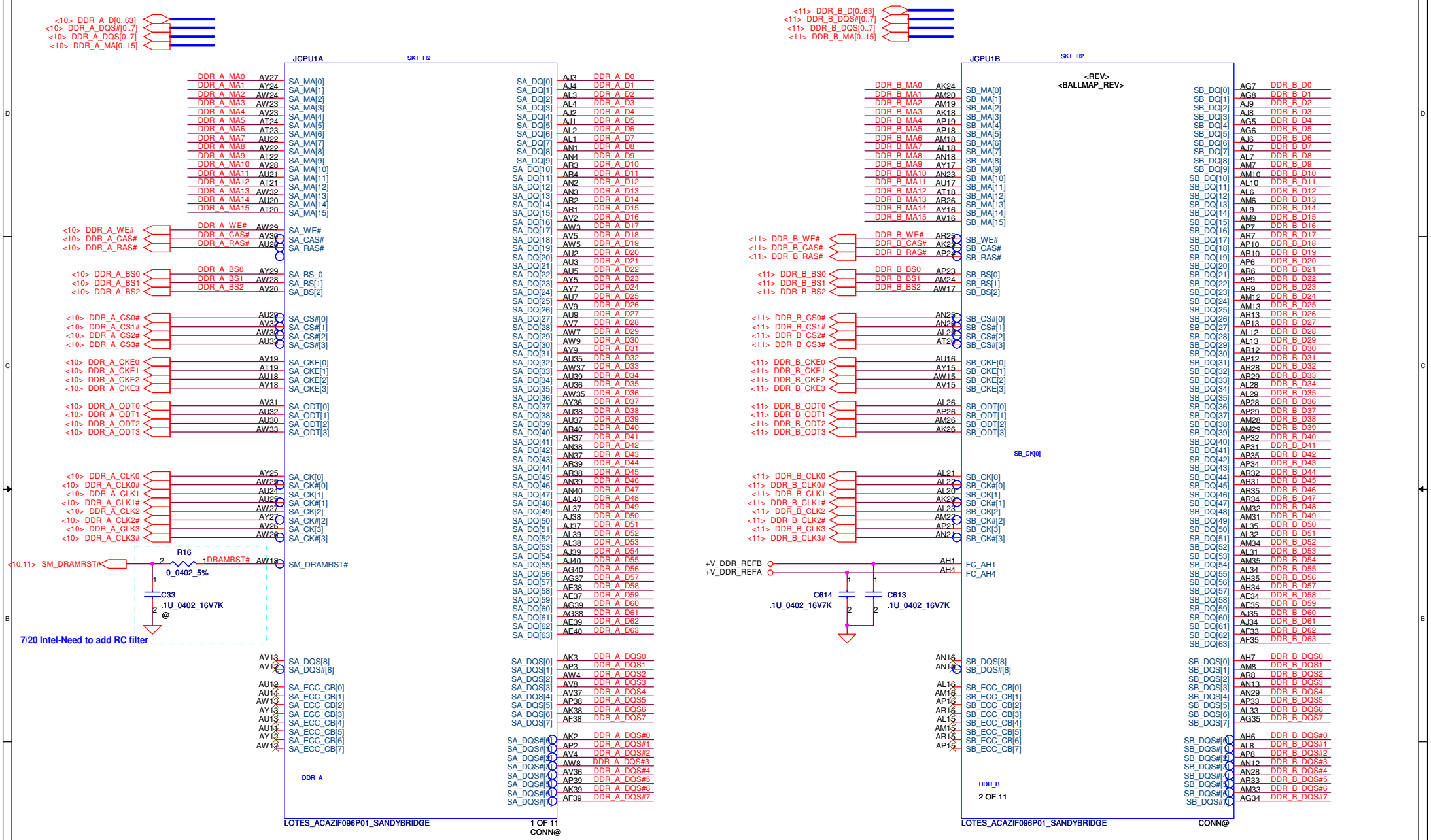
Compal Electronics, Inc.
Title
PROCESSOR (2/6) CLK,JTAG
Size
B
Document Number
PLA00 M/B LA-6951P Schematic
Rev
0.3
Date:
Friday, November 05, 2010
Sheet
5
of
62



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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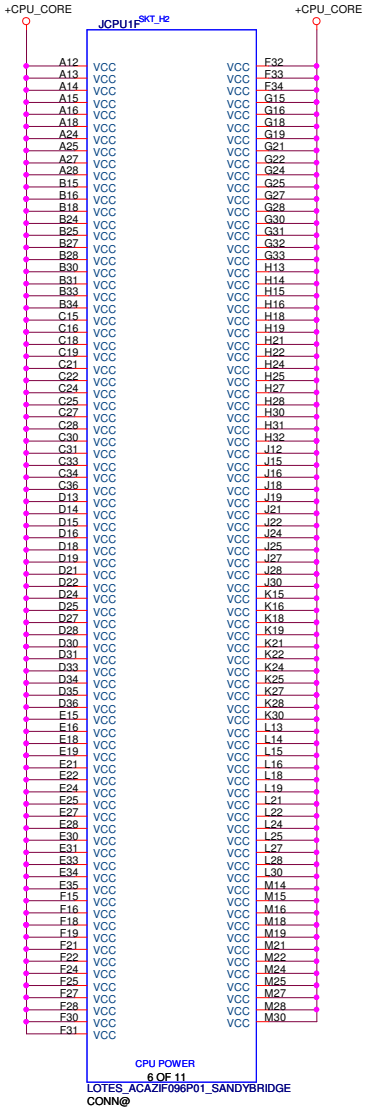
Compal Electronics, Inc.

Title: PROCESSOR (3/6) DDRIII

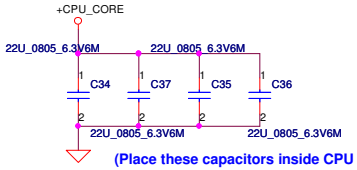
Size	Document Number	Rev
B	PLA00 M/B LA-6951P Schematic	0.3

Date: Friday, November 05, 2010 | Sheet 6 of 62

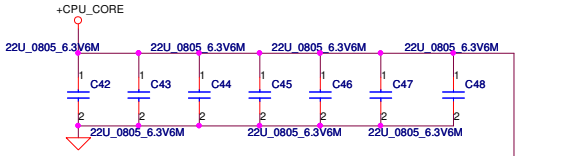
+CPU_CORE : 112A



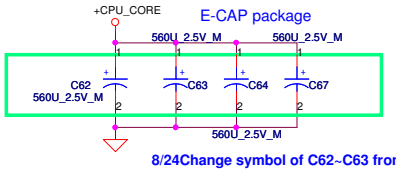
+CPU_CORE

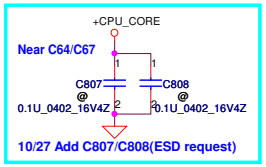


(Place these capacitors inside CPU socket cavity, top layer)



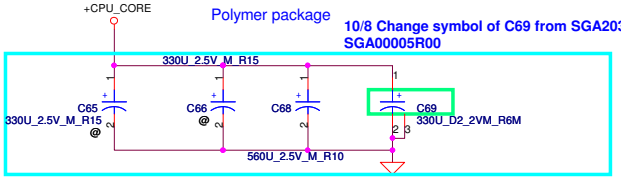
(Place these capacitors under CPU socket, Bottom layer)





8/24Change symbol of C62~C63 from SF000001P00 to SF000001K00

(Place C62~C64 capacitors under CPU socket, Top layer)

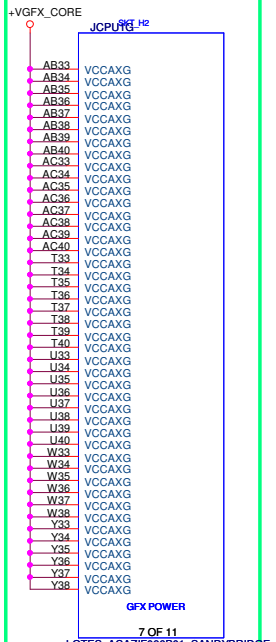


10/8 Change symbol of C69 from SGA20331E10 to SGA00005R00

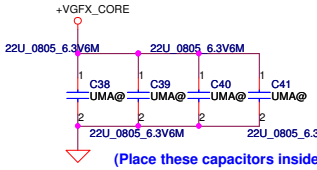
10/23 Change symbol of C65/C66/C68 from SGA20331E10 to SF000002M00
(Place C65~C69 capacitors under CPU socket, Bottom layer)

11/2 Change PN of C68 from SF000002M00 to SF000001K00

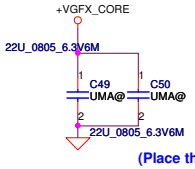
+VGFX_CORE : 35A



+VGFX_CORE

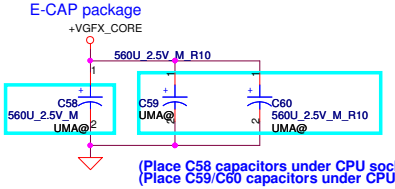


(Place these capacitors inside CPU socket cavity, top layer)



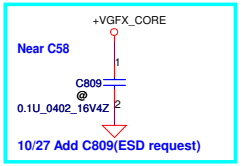
(Place these capacitors under CPU socket, Bottom layer)

E-CAP package



(Place C58 capacitors under CPU socket, Top layer)
(Place C59/C60 capacitors under CPU socket, Bottom layer)

8/24Change symbol of C58 from SF000001P00 to SF000001K00
10/23 Change symbol of C59/C60 from SGA20331E10 to SF000002M00
11/2 Change PN of C59/C60 from SF000002M00 to SF000001K00



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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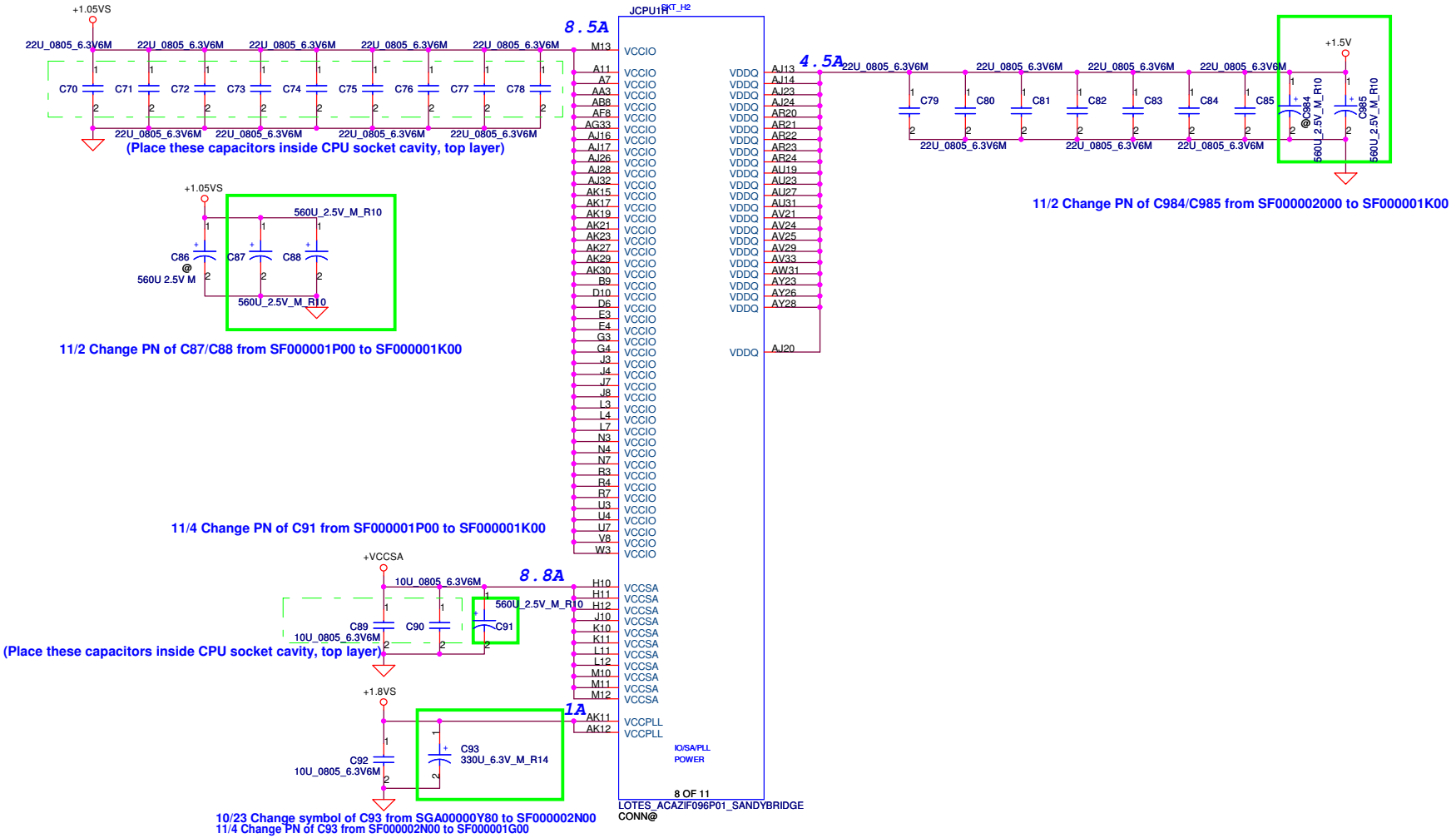
Compal Electronics, Inc.

Title: PROCESSOR (4/6) PWR,Bypass

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

Date: Thursday, November 04, 2010 | Sheet 7 of 62



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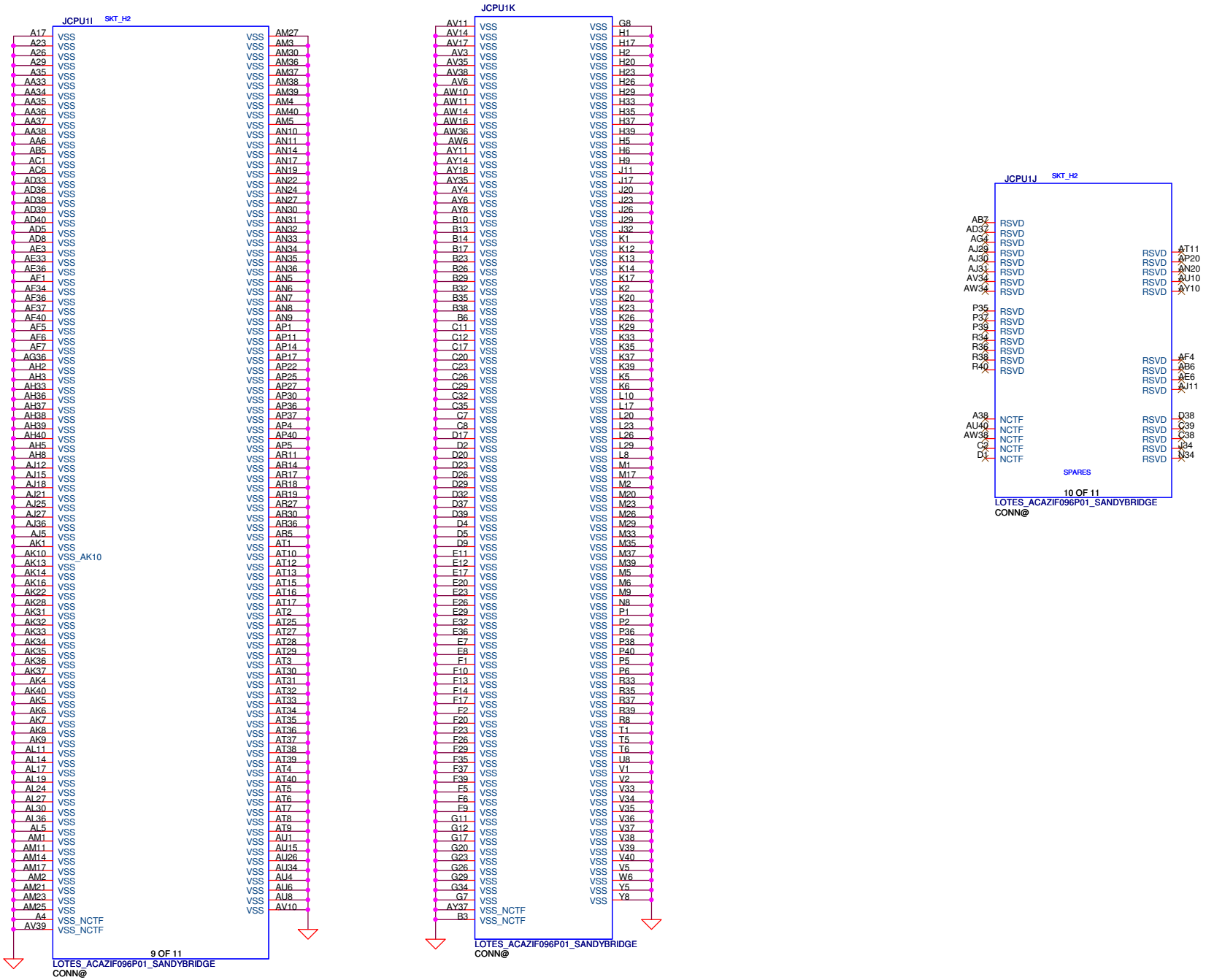
Compal Electronics, Inc.

Title: PROCESSOR (5/6) PWR

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.3

Date: Thursday, November 04, 2010 | Sheet 8 of 62



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Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Compal Electronics, Inc.

Title: PROCESSOR (6/6) VSS

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.3

Date: Thursday, November 04, 2010 Sheet 9 of 62

Layout Note:Place C94 on Bottom Layer at DIMM close to CPU

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMMA

Layout Note: Place near JDIMMA

10/23 Change symbol of C107 from SGA20331E10 to SF000002M00

Layout Note:Place near JDIMM1.203/204

Layout Note:Place near JDIMM2.203/204

STANDARD:9.2mm

STANDARD:5.2mm

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Compal Electronics, Inc.

Title: DDRIII CHANNELA

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

Date: Friday, November 05, 2010 | Sheet 10 of 62

Layout Note:Place C124 on Bottom Layer at DIMM close to CPU

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMMB

Layout Note: Place near JDIMMB

10/23 Change symbol of C129 from SGA20331E10 to SF000002M00
11/2 Change PN of C129 from SF000002M00 to SF000001K00

Layout Note:Place near JDIMM4.203/204

Layout Note:Place near JDIMM3.203/204

<Address: 01>

Reverse H:5.2mm

Reverse H:9.2mm

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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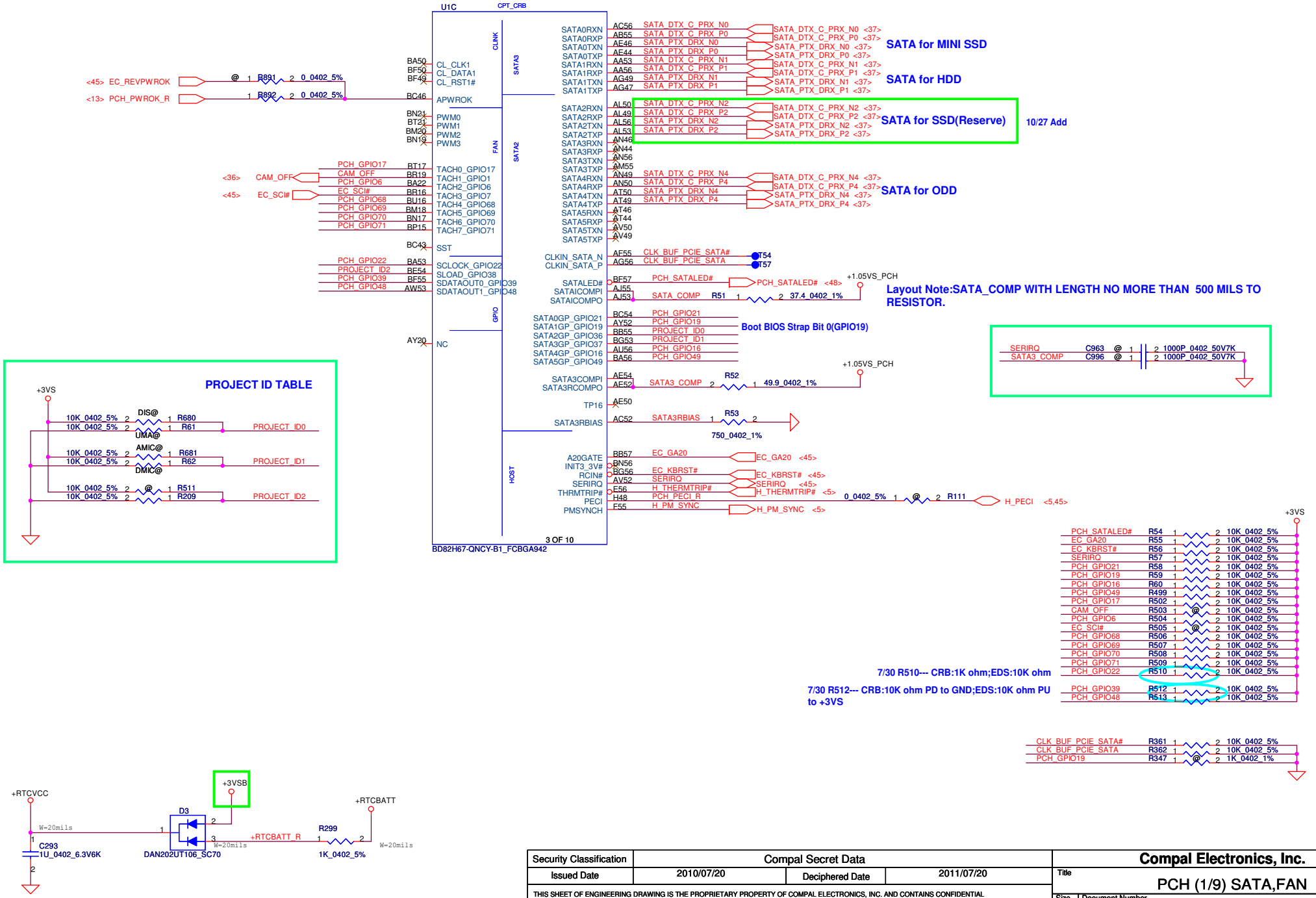
Compal Electronics, Inc.

Title: DDRIII CHANNELB

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.3

Date: Friday, November 05, 2010 | Sheet 11 of 62



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Compal Electronics, Inc.			
Title	PCH (1/9) SATA,FAN		
Size: Custom	Document Number: PLA00 M/B LA-6951P Schematic		Rev: 0.3
Date: Friday, November 05, 2010	Sheet 12 of 62		

HDA for AUDIO

<41> HDA_BITCLK_AUDIO — R69 33_0402_5% — HDA_BITCLK_PCH
<41> HDA_RST#_AUDIO — R72 33_0402_5% — HDA_RST#_PCH
<41> HDA_SDOUT_AUDIO — R73 33_0402_5% — HDA_SDOUT_PCH

HDA_SDO
ME debug mode,
this signal has a weak internal pull down
★Low = Disable (default)
High = Enable (flash descriptor security overide)

HDA_SYNC
This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
★Need to pull high for Huron River platform

<41> HDA_SYNC_AUDIO — R70 33_0402_5% — HDA_SYNC_AUDIO_R
@ R356 1M_0402_5%

PCH_RSMRST# R303 0_0402_5% PCH_DPWROK
Stuff R303 if do not support DeepSX state
EC_PWROK R344 0_0402_5% PCH_PWROK_R

<21,42,45> EC_SMB_CK2 — R88 0_0402_5% — EC_SMB_CK2
<21,42,45> EC_SMB_DA2 — R89 0_0402_5% — EC_SMB_DA2

C146 18P_0402_50V8J
X1 32.768KHZ_12.5PF_Q13MC1460002
C147 18P_0402_50V8J
R87 10M_0402_5%
PCH_RTCX1
PCH_RTCX2

8/20 Add
1000P_0402_50V7K C987 LAN_CLKREQ#
1000P_0402_50V7K C988 PCH_JTAG_TDO

+RTCVCC close to RAM door
R99 20K_0402_1% PCH_SRTCRST#
J2 10K_0603_5%
C149 1U_0402_6.3V6K
RC Delay 18~25mS

+3VS
R655 4.7K_0402_5%
PCH_SMBCLK — D_CK_SCLK — D_CK_SCLK <10,11>
Q32 SSM3K7002FU_SC70-3

+RTCVCC close to RAM door
R90 20K_0402_1% PCH_RTCRST#
J1 10K_0603_5%
C148 1U_0402_6.3V6K
RC Delay 18~25mS

+3VS
R654 4.7K_0402_5%
PCH_SMBDATA — D_CK_SDATA — D_CK_SDATA <10,11>
Q31 SSM3K7002FU_SC70-3

+RTCVCC
1M_0402_5% R103 SM_INTRUDER#
390K_0402_5% R104 PCH_DSWVRMEN
390K_0402_5% R105 PCH_INTVRMEN
R106 1K_0402_5% @

+3VALW
R338 1K_0402_1% @
<45> ME_FLASH — R890 0_0402_5% — HDA_SDOUT_PCH / HDA_SYNC_AUDIO_R

PCH_SPI_MOSI_1 R79 0_0402_5% PCH_SPI_MOSI
PCH_SPI_MISO_1 R80 0_0402_5% PCH_SPI_MISO
PCH_SPI_CS0# R81 0_0402_5% PCH_SPI_CS0#_R
PCH_SPI_CLK_1 R83 0_0402_5% PCH_SPI_CLK

+3VALW
2.2K_0402_5% R945 PCH_SMBCLK
2.2K_0402_5% R946 PCH_SMBDATA

<12> PCH_PWROK_R

<37,44> PCH_SMBCLK
<37,44> PCH_SMBDATA
<40> LAN_SMBCLK
<40> LAN_SMBDATA

<45> LPC_AD0 — LPC_AD0
<45> LPC_AD1 — LPC_AD1
<45> LPC_AD2 — LPC_AD2
<45> LPC_AD3 — LPC_AD3
<45> LPC_FRAME# — LPC_FRAME#
HDA_BITCLK_PCH
HDA_RST#_PCH
<41> HDA_SDIN0 — HDA_SDIN0

U1D

BA20	LDRQ1#_GPIO23	BMBUSY#_GPIO0	AW55 PCH_GPIO0
BK15	FWH0_LAD0	CLKRUN#_GPIO32	BC56 CLKRUN# — CLKRUN# <45>
BJ17	FWH1_LAD1	HDA_DOCK_EN#_GPIO33	BC25 PCH_GPIO33
BJ20	FWH2_LAD2	STP_PCI#_GPIO34	BL56 PCH_GPIO34
BG20	FWH3_LAD3	GPIO35	BJ57 PCH_GPIO35
BK17	LDRQ0#		
BG17	FWH4_LFRAME#	GPIO8	BP51 EC_SMI# — EC_SMI# <38,45>
		LAN_PHY_PWR_CTRL_GPIO12	BK50 PM_LANPHY_ENABLE — PM_LANPHY_ENABLE <40>
		HDA_DOCK_RST#_GPIO13	BA25 PCH_GPIO13
BU22	HDA_BCLK	GPIO15	BM55 SMIB — SMIB <38>
BC22	HDA_RST#	GPIO24_MEM_LED	BR53 T1
BD22	HDA_SDIN0	GPIO28	BJ55 PCH_GPIO28
BF22	HDA_SDIN1	SLP_LAN#_GPIO29	BH49 SLP_LAN# — SLP_LAN# <40>
BK22	HDA_SDIN2	PCIECLKRQ2#_GPIO20	AV43 LAN_CLKREQ# — LAN_CLKREQ# <40>
BJ22	HDA_SDIN3	PCIECLKRQ5#_GPIO44	BL54 WLAN_CLKREQ# — WLAN_CLKREQ# <44>
BT23	HDA_SDO	PCIECLKRQ6#_GPIO45	AV44 CLKREQ_USB30# — CLKREQ_USB30# <38>
BP23	HDA_SYNC	PCIECLKRQ7#_GPIO46	BP55 TV_CLKREQ# — TV_CLKREQ# <44>
		GPIO57	BT53 PCH_GPIO57
AU53	SPI_MOSI	SYS_PWROK	BJ53 SYS_PWROK_R
AT55	SPI_MISO	RI#	BJ48 EC_SWI# — EC_SWI# <45>
AT57	SPI_CS0#	PLTRST#	BK48 PCH_PLT_RST# — PCH_PLT_RST# <5,40,45>
AR54	SPI_CLK	WAKE#	BC44 PCH_PCIE_WAKE# R — R364 0_0402_5% — PCH_PCIE_WAKE# <38,44>
AR56	SPI_CS1#	SLP_A#	BC41
		SLP_S3#	BM53 PM_SLP_S3# — PM_SLP_S3# <45>
		SLP_S4#	BN52 PM_SLP_S4# — PM_SLP_S4# <45>
		SLP_S5#_GPIO63	BH50 PM_SLP_S5# — PM_SLP_S5# <45>
		SUS_STAT#_GPIO61	BN54 T2
		SUSCLK_GPIO62	BA47 PCH_SUSCLK_R — R363 0_0402_5% — PCH_SUSCLK <45>
		BATLOW#_GPIO72	AV46 PCH_GPIO72
		SUSACK#	BP45 SUS_PWR_ACK_R — R365 0_0402_5% — SUS_PWR_ACK <45>
BR39	RTCX1	SUSWARN#-SUS_PWR_DN_ACK-GPIO30	BU46 SUSWARN# R — R390 0_0402_5% — SUSWARN# <45>
BN39	RTCX2	DRAMPWROK	BG46 DRAMPWROK — DRAMPWROK <5>
BT41	RTCRST#		
BN37	SRTCRST#	GPIO27	BJ43 PCH_GPIO27
BM38	INTRUDER#		
BJ38	PWROK	GPIO31	BG43 PCH_GPIO31
BK38	RSMRST#	SLP_SUS#	BD43 T51
BN41	INTVRMEN	PWRBTN#	BT43 PBTN_OUT# — PBTN_OUT# <45>
BT37	DPWROK		
BR42	DSWVRMEN	SYS_RESET#	BE52 XDP_DBRETSET# — XDP_DBRETSET# <5>
		SPKR	BE56 PCH_SPKR — PCH_SPKR <41>
BN49	SMBALERT#_GPIO11		
BT47	SMBCLK	PROCPWRGD	D53 H_CPUPWRGD — H_CPUPWRGD <5>
BR49	SMBDATA		
BU49	SML0ALERT#_GPIO60		
BT51	SML0CLK		
BM50	SML0DATA		
BR46	SML1ALERT#_PCHHOT#_GPIO74		
BJ46	SML1CLK_GPIO58		
BK46	SML1DATA_GPIO75		
		TP12	BC49 PCH_JTAG_RST#
		JTAG_TCK	BA43 PCH_JTAG_TCK
		JTAG_TDI	BC52 PCH_JTAG_TDI
		JTAG_TDO	BF47 PCH_JTAG_TDO
		JTAG_TMS	BC50 PCH_JTAG_TMS

PM_GPIO0(SW)
JTAG(SUS)
4 OF 10
BD82H67-QNCY-B1_FCBGA942

PCH_GPIO11 BN49
PCH_SMBCLK BT47
PCH_SMBDATA BR49
PCH_GPIO60 BU49
LAN_SMBCLK BT51
LAN_SMBDATA BM50
PCH_GPIO74 BR46
PCH_SML1CLK BJ46
PCH_SML1DAT BK46

PCH_RTCX1 BR39
PCH_RTCX2 BN39
PCH_RTCRST# BT41
PCH_SRTCRST# BN37
SM_INTRUDER# BM38
PCH_PWROK_R BJ38
PCH_RSMRST# BK38
PCH_INTVRMEN BN41
PCH_DPWROK BT37
PCH_DSWVRMEN BR42

8/19 Change footprint of U2 to WIESO_G6179-100000_8P
SA000041P00 4MB
U2
CS# VCC
WP# SCLK
HOLD# SI
GND SO
S IC FL 32M MX25L3206EM2I-12G SOP 8P
SPI ROM Footprint 200mil
R94 4.7K_0402_5% SPI_WP1#
R96 4.7K_0402_5% SPI_HOLD1#
PCH_SPI_CS0# — PCH_SPI_CLK_1 — PCH_SPI_MOSI_1 — PCH_SPI_MISO_1

R348 0_0402_5%
U20 NC7SZ08P5X_NL_SC70-5
SYS_PWROK — EC_PWROK — EC_PWROK <45>
VGATE — VGATE <45,57>

R943 0_0402_5%
U25 NC7SZ08P5X_NL_SC70-5
PCH_PLT_RST# — PLT_RST# — PLT_RST# <22,38,39,44>
R944 100K_0402_5%

SYS_PWROK_R — R349 0_0402_5% — SYS_PWROK
R350 0_0402_5% — VGATE

R342 0_0402_5%
Q18 MMBT3906_SOT23-3
PCH_RSMRST# — EC_RSMRST# <45>
R717 10K_0402_5%
R319 4.7K_0402_5% — +3VALW
D38A D38B BAV99DW-7-F_SOT363-N
R343 2.2K_0402_5%

+3VALW
EC_SMI# R324 10K_0402_5%
EC_SWI# R74 10K_0402_5%
PCH_GPIO74 R75 10K_0402_5%
PCH_SML1CLK R63 4.7K_0402_5%
PCH_SML1DAT R76 4.7K_0402_5%
LAN_SMBCLK R64 2.2K_0402_5%
LAN_SMBDATA R65 2.2K_0402_5%
PCH_GPIO60 R77 2.2K_0402_5%
PM_LANPHY_ENABLE R66 10K_0402_5%
SMIB R67 10K_0402_5%
PCH_GPIO28 R68 1K_0402_1%
PCH_GPIO13 R896 10K_0402_5%
SUSWARN#_R R448 10K_0402_5%
PCH_GPIO57 R71 10K_0402_5%
PCH_GPIO27 R78 10K_0402_5%
WLAN_CLKREQ# R530 10K_0402_5%
CLKREQ_USB30# R531 10K_0402_5%
TV_CLKREQ# R532 10K_0402_5%
DRAMPWROK R646 200_0402_5%
PCH_GPIO31 R675 10K_0402_5%
PCH_GPIO72 R676 200_0402_5%
PCH_PCIE_WAKE# R R203 1K_0402_1%
PCH_GPIO11 R716 10K_0402_5%

SUS_PWR_ACK_R R391 0_0402_5% SUSWARN#_R
Stuff R391 if EC don't want to involve in the handshake mechanism for the DeepSX state entry and exit

+3VS
PCH_GPIO33 R894 10K_0402_5%
PCH_GPIO0 R82 10K_0402_5%
PCH_GPIO34 R84 10K_0402_5%
LAN_CLKREQ# R529 10K_0402_5%
XDP_DBRETSET# R581 10K_0402_5%
PCH_SPKR R583 1K_0402_5%
PCH_SPKR:HIGH= Enable (No Reboot);
★LOW= Disable(Default)

CLKRUN# R926 10K_0402_5%
SLP_LAN# R897 1K_0402_1%
PCH_GPIO33 R895 1K_0402_1%
SYS_PWROK R719 10K_0402_5%
PCH_GPIO35 R85 2.2K_0402_5%
EC_SMI# R86 1K_0402_1%
SUSWARN# R R207 1K_0402_1%
EC_PWROK R718 10K_0402_5%
PCH_GPIO28 R340 1K_0402_1%
★On-Die PLL Voltage Regulator
H: Enable
L: Disable

XDP_DBRETSET# C676 0.1U_0402_16V4Z <EMI>
8/13 Add C676 close to U1(EMI request)

+3VALW
PCH_JTAG_TMS R91 200_0402_5% R92 100_0402_5%
PCH_JTAG_TDO R93 200_0402_5% R95 100_0402_5%
PCH_JTAG_TDI R97 200_0402_5% R98 100_0402_5%
PCH_JTAG_RST# R100 20K_0402_5% R101 10K_0402_5%
PCH_JTAG_TCK R102 51_0402_5%

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Issued Date	2010/07/20	Deciphered Date	2011/07/20

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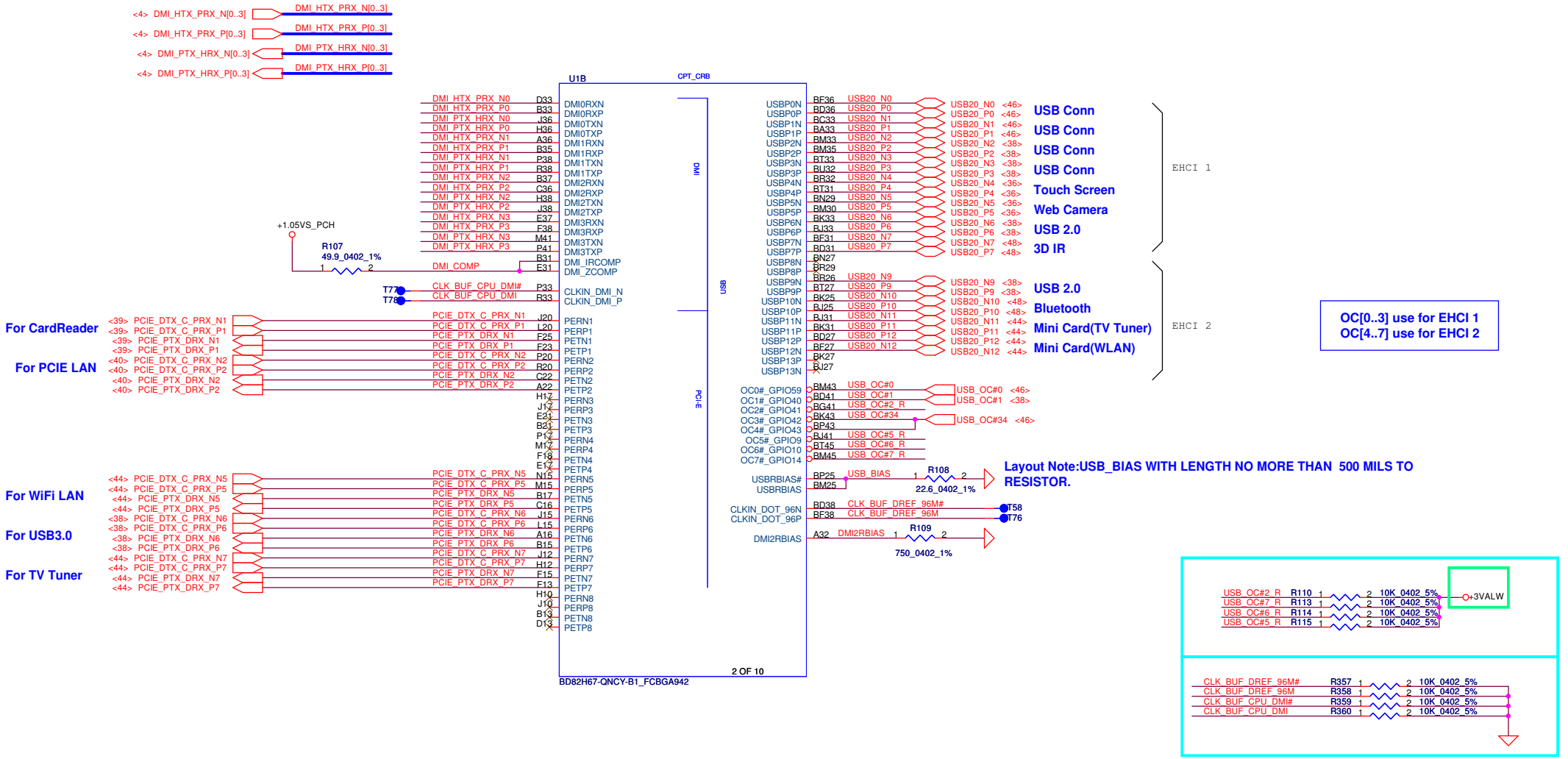
Compal Electronics, Inc.

Title	PCH (2/9) LPC, HDA, SMBUS	
Size: Custom	Document Number: PLA00 M/B LA-6951P Schematic	Rev: 0.3
Date: Friday, November 05, 2010	Sheet 13 of 62	



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Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Compal Electronics, Inc.

Title: PCH (3/9) DMI, USB, PCIE

Size	Document Number	Rev
A	PLA00 M/B LA-6951P Schematic	0.3

Date: Friday, November 05, 2010 Sheet 14 of 62

PLACE RGB RESISTORS CLOSE TO PCH:<250 MILS TO MCH BALL

PLACE DACREFSET RES(R121) CLOSE TO PCH:<500 MILS TO MCH BALL

For HDMI OUT

DMI & FDI Termination Voltage	
NV_CLE	Set to VCC when HIGH
	Set to VSS when LOW

Note:Place R637 close to U1.R47 and <=100 mils

11/4 Change PN of Q15 from SB00000AR00 to SB00000DH00

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Issued Date	2010/07/20	Deciphered Date	2011/07/20

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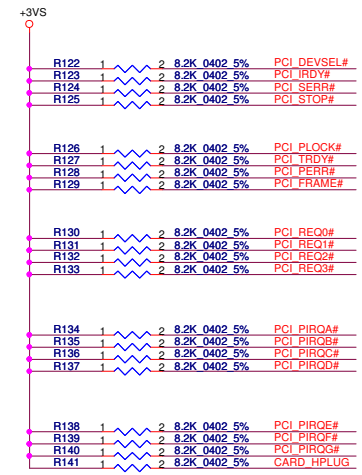
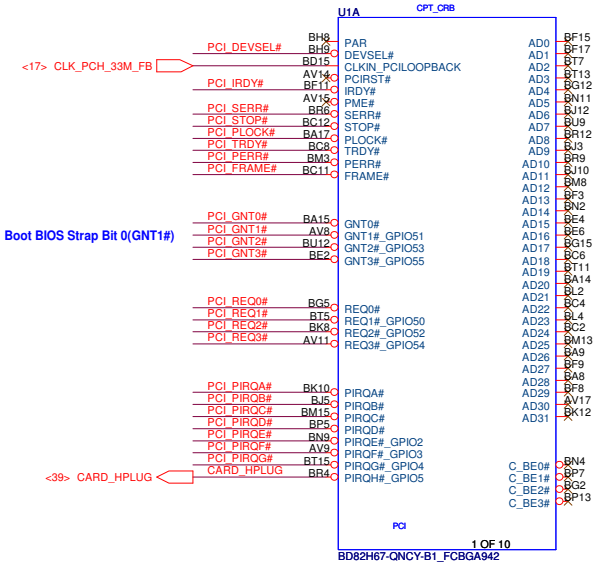
Compal Electronics, Inc.

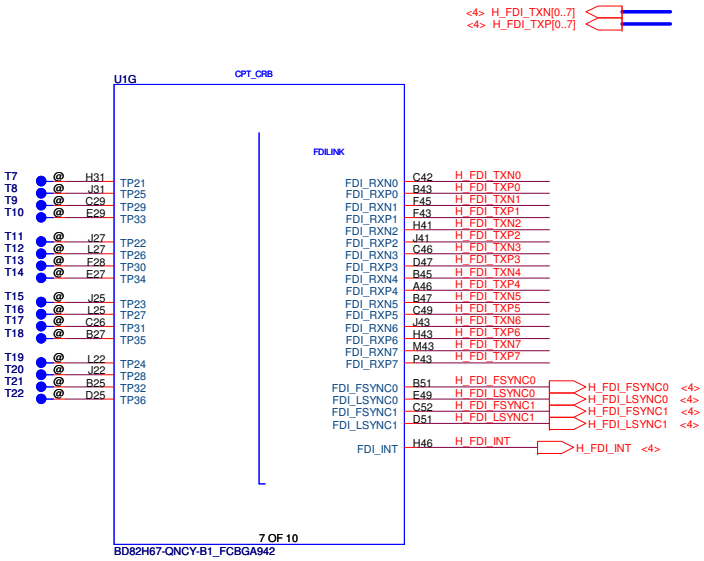
Title: PCH (4/9) CRT, DPI, VRAM

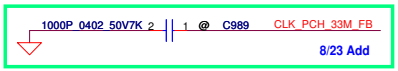
Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

Date: Friday, November 05, 2010 | Sheet 15 of 62

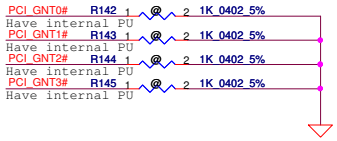








Boot BIOS Strap		
PCH_GNT1#	PCH_GPIO19	Boot BIOS Loaction
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI ★



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Compal Electronics, Inc.

Title: PCH (5/9) PCI,FDI

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.3

Date: Friday, November 05, 2010 Sheet 16 of 62

Security Classification	Compal Secret Data		
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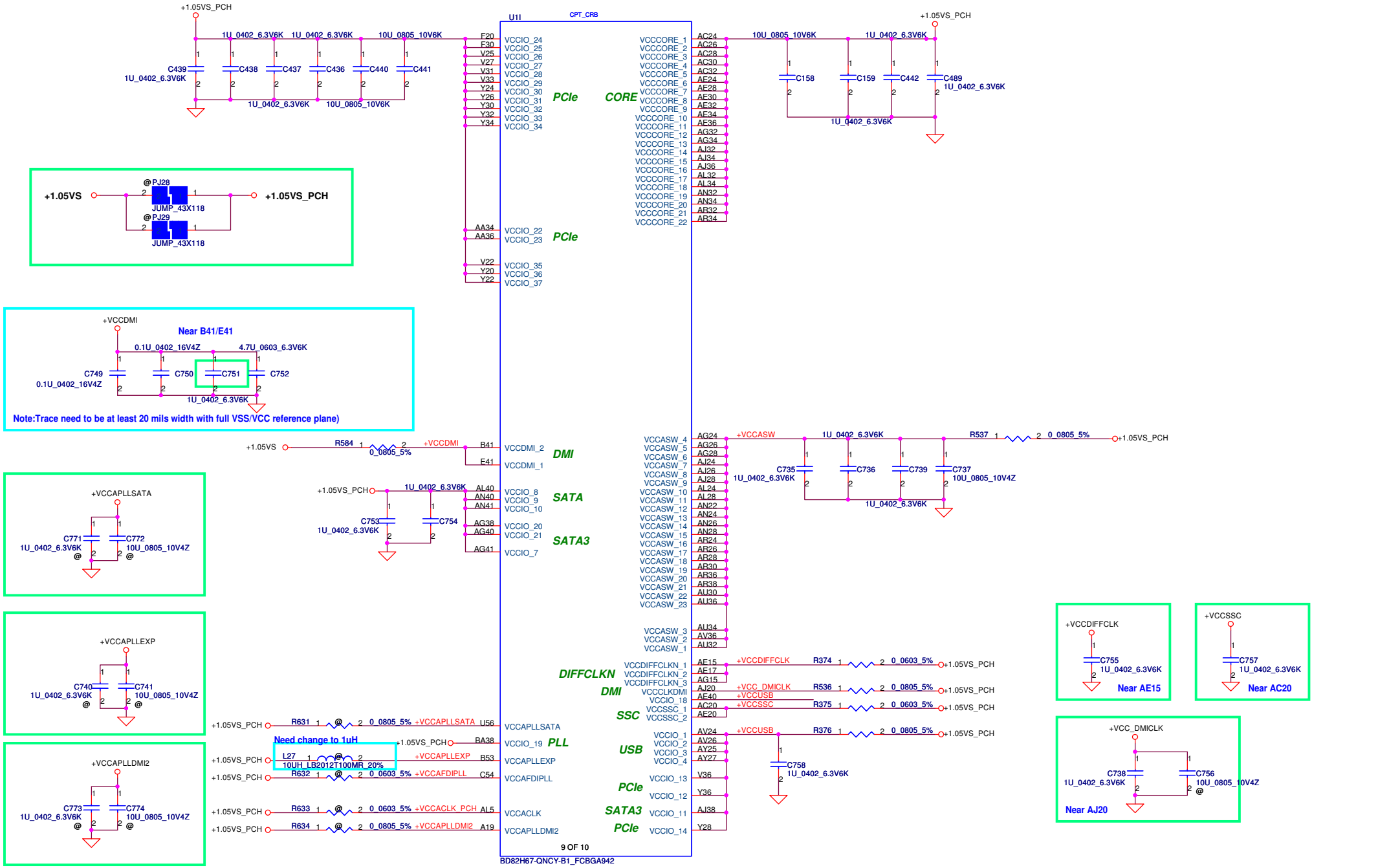
Compal Electronics, Inc.

Title: PCH (6/9) CLOCK

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.3

Date: Friday, November 05, 2010 Sheet 17 of 62



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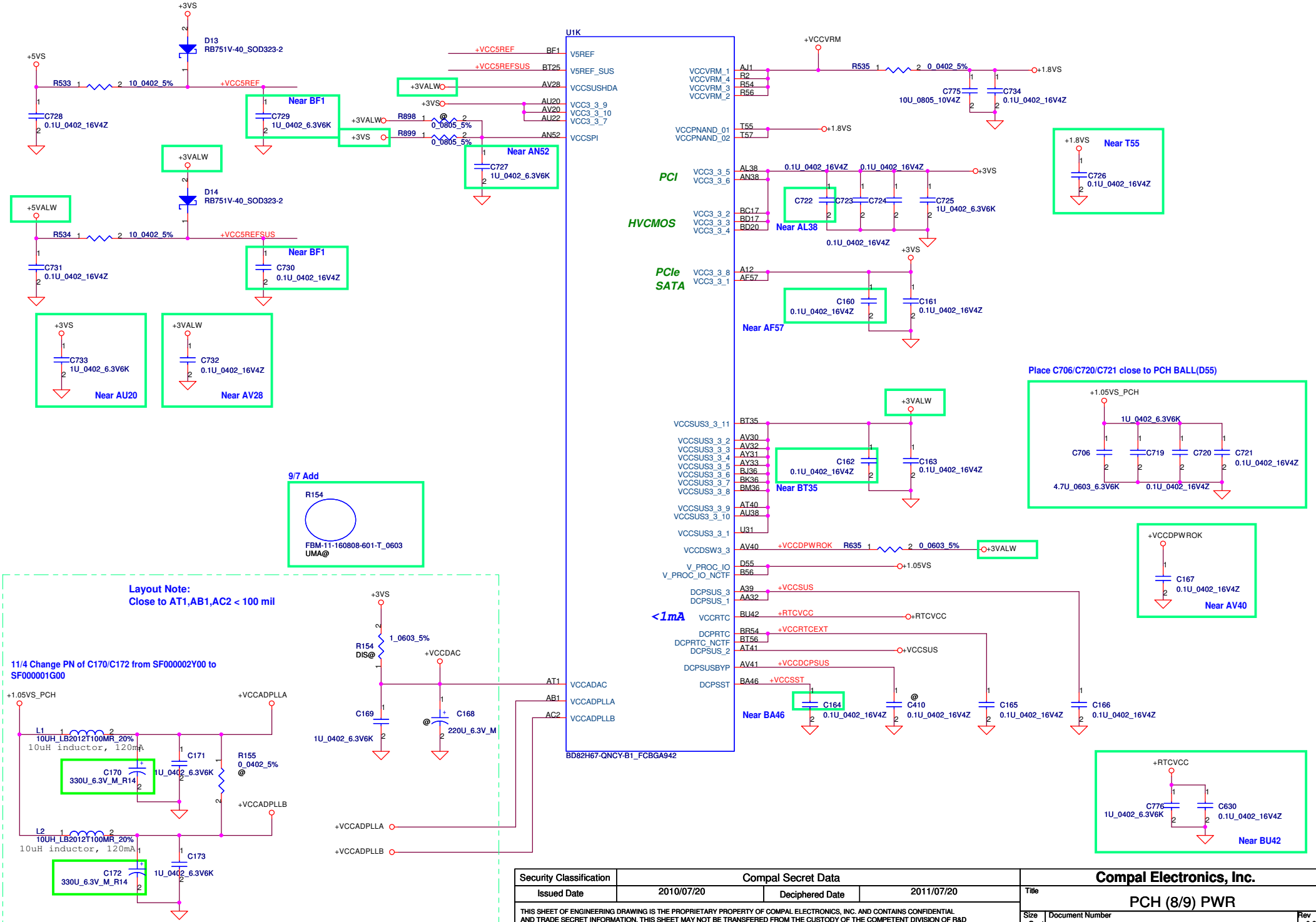
Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

Date: Friday, November 05, 2010 | Sheet 18 of 62



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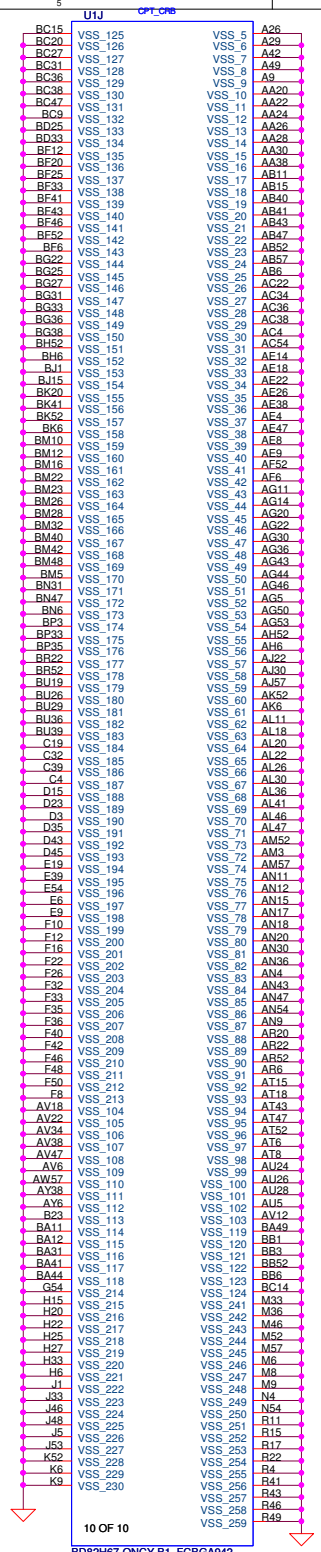
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.3

Date: Friday, November 05, 2010 Sheet 19 of 62



NOTE:PCH adds support for panel power sequencing required for embedded DisplayPort support. L_VDDEN, L_BKLTEN and L_BKLTCTL pins are added on the PCH for panel power sequencing. It is important to note that a 6 layer board design may be required to access these pins on the PCH package in a fully featured platform design.

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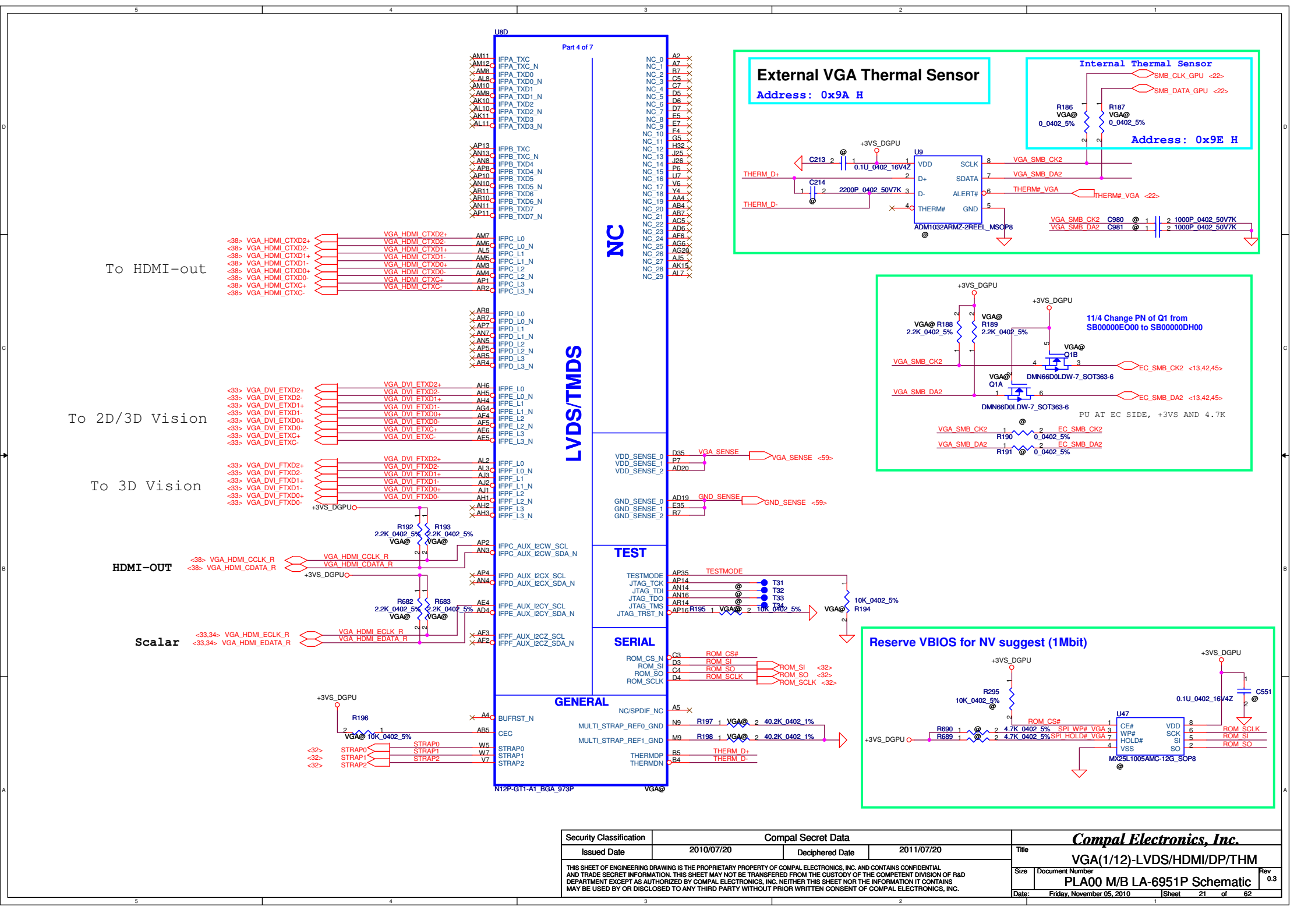
Compal Electronics, Inc.

Title: **PCH(9/9)VSS**

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.3

Date: Friday, November 05, 2010 | Sheet 20 of 62



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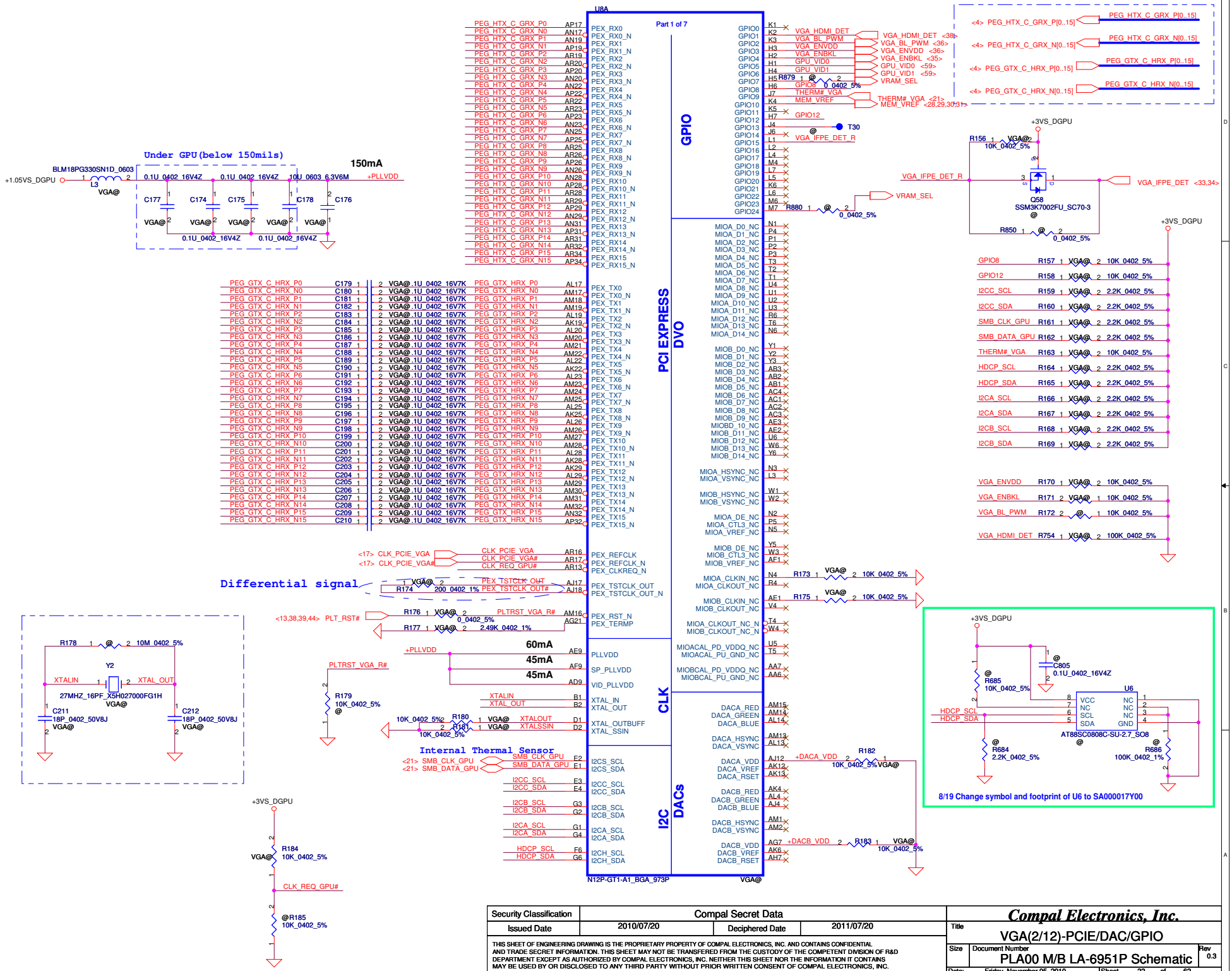
Compal Electronics, Inc.

Title: VGA(1/12)-LVDS/HDMI/DP/THM

Size	Document Number	Rev
	PLA00 M/B LA-6951P Schematic	0.3

Date: Friday, November 05, 2010 | Sheet 21 of 62



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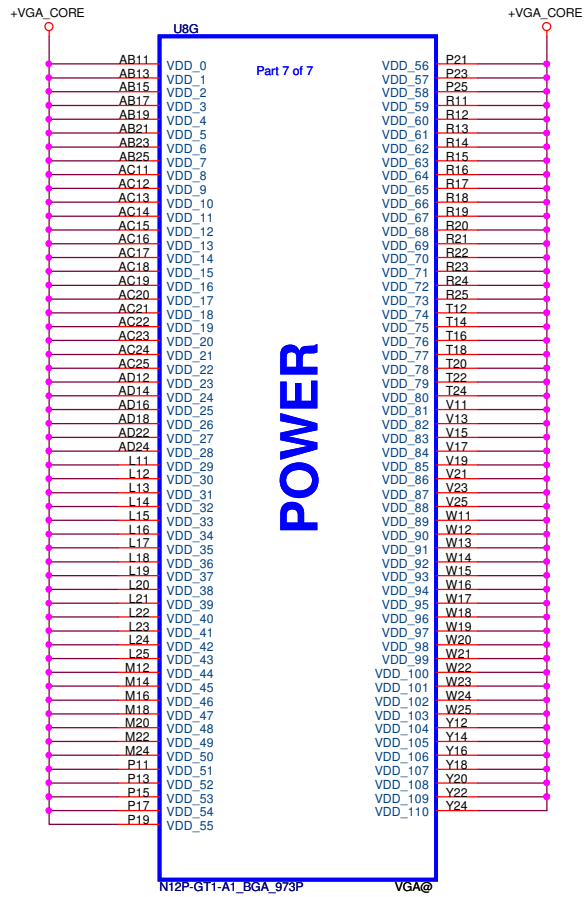
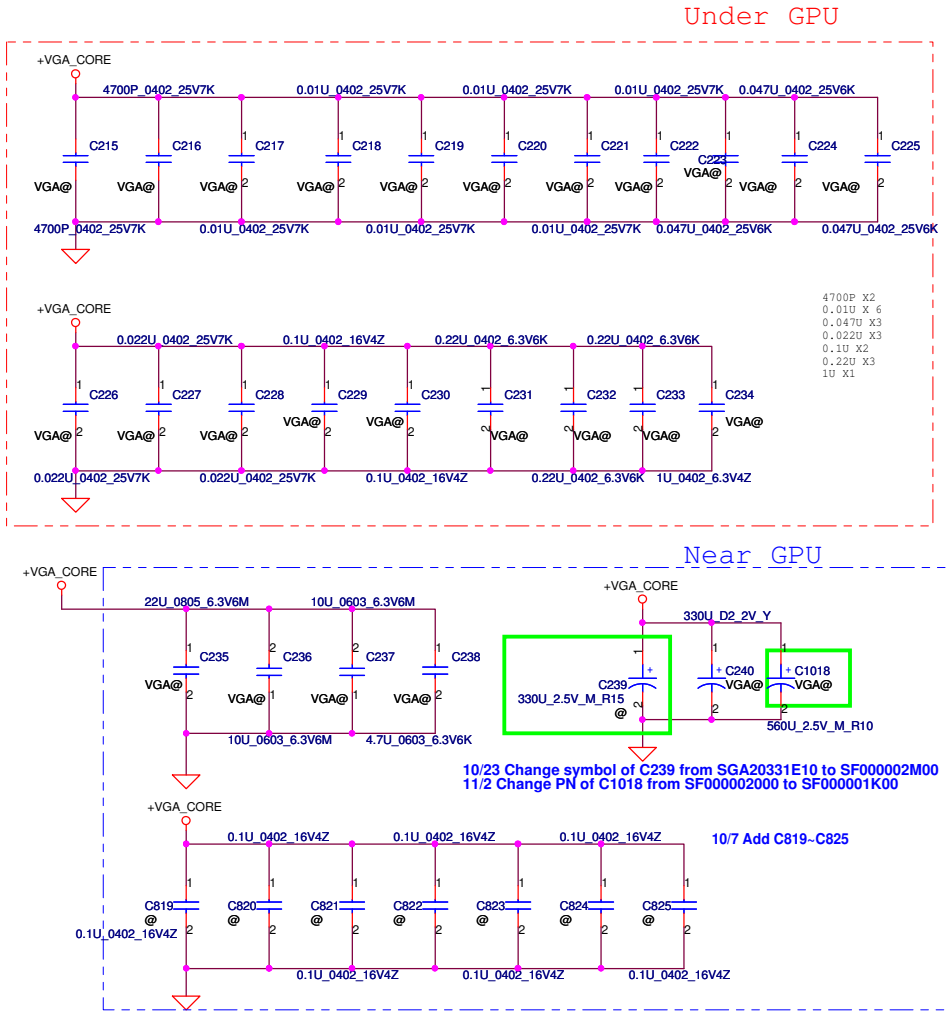
Compal Electronics, Inc.

Title: VGA(2/12)-PCIE/DAC/GPIO

Size: | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

Date: Friday, November 05, 2010 | Sheet 22 of 62





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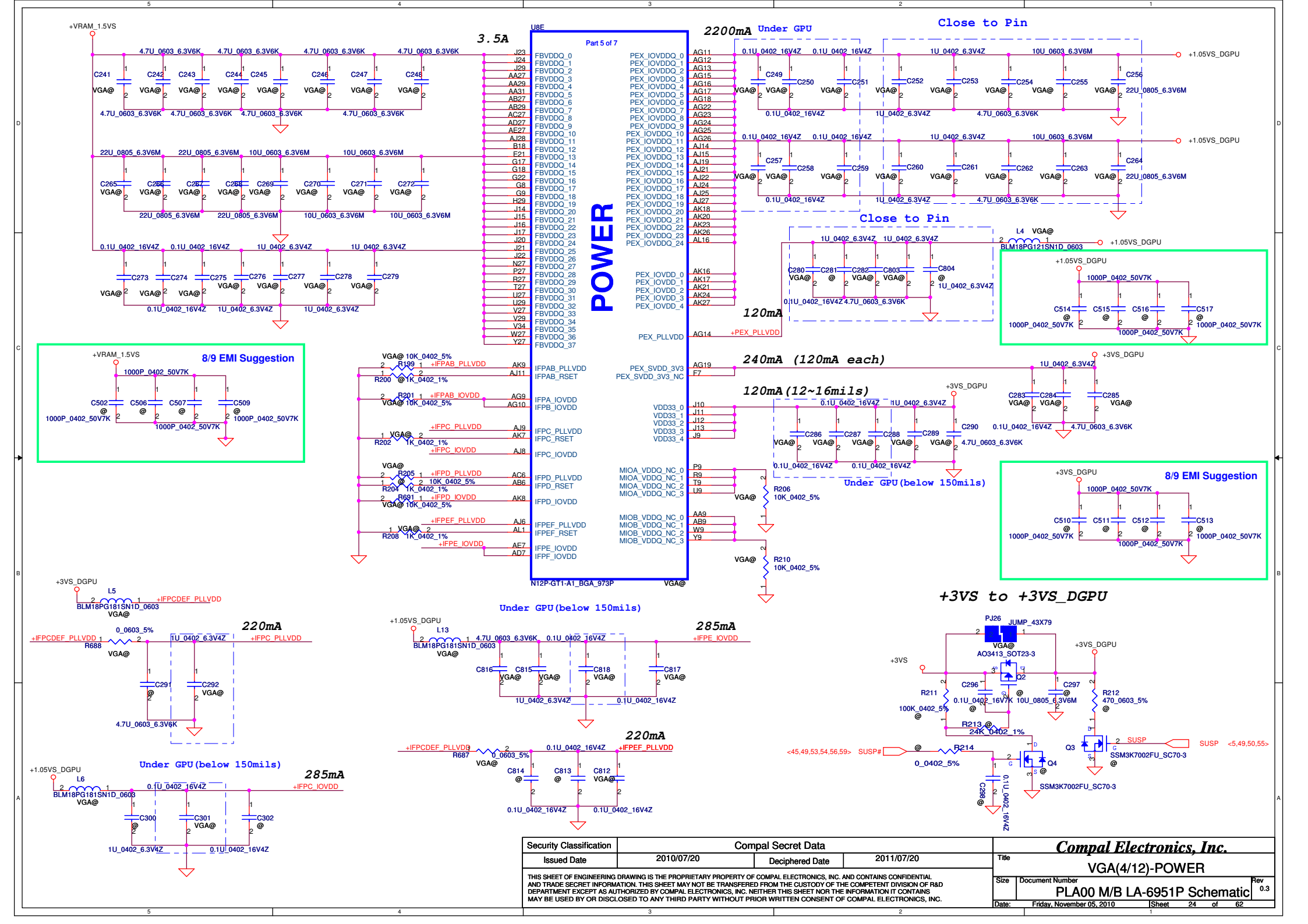
Compal Electronics, Inc.

Title: VGA(3/12)-VGA CORE

Size	Document Number	Rev
	PLA00 M/B LA-6951P Schematic	0.3

Date: Thursday, November 04, 2010 | Sheet 23 of 62


POWER
Part 5 of 7
U8E
N12P-GT1-A1_BGA_973P
3.5A
2200mA
Under GPU
Close to Pin
120mA
240mA (120mA each)
120mA(12~16mils)
Under GPU(below 150mils)
8/9 EMI Suggestion
+3VS to +3VS_DGPU
220mA
285mA
+VRAM_1.5VS
+1.05VS_DGPU
+3VS_DGPU
+IFPC_PLLVDD
+IFPC_IOVDD
+IFPE_IOVDD
+IFPEF_PLLVDD
+IFPCDEF_PLLVDD
+PEX_PLLVDD
SUSP
SUSP#
Security Classification
Compal Secret Data
Issued Date
2010/07/20
Deciphered Date
2011/07/20
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Title
VGA(4/12)-POWER
Size
Document Number
PLA00 M/B LA-6951P Schematic
Rev
0.3
Date:
Friday, November 05, 2010
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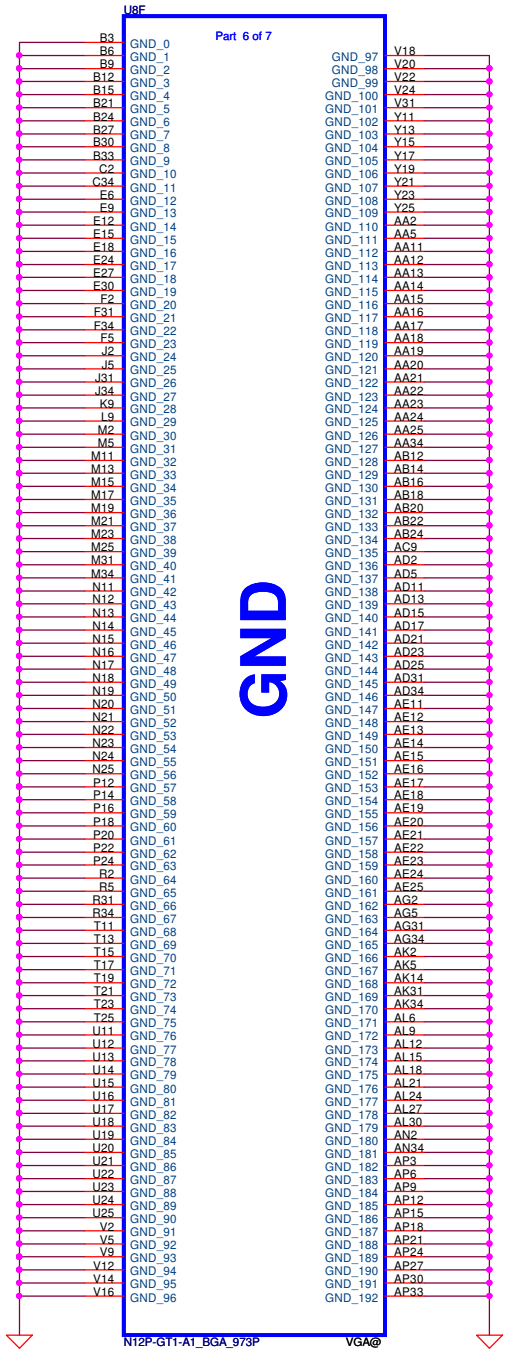
62



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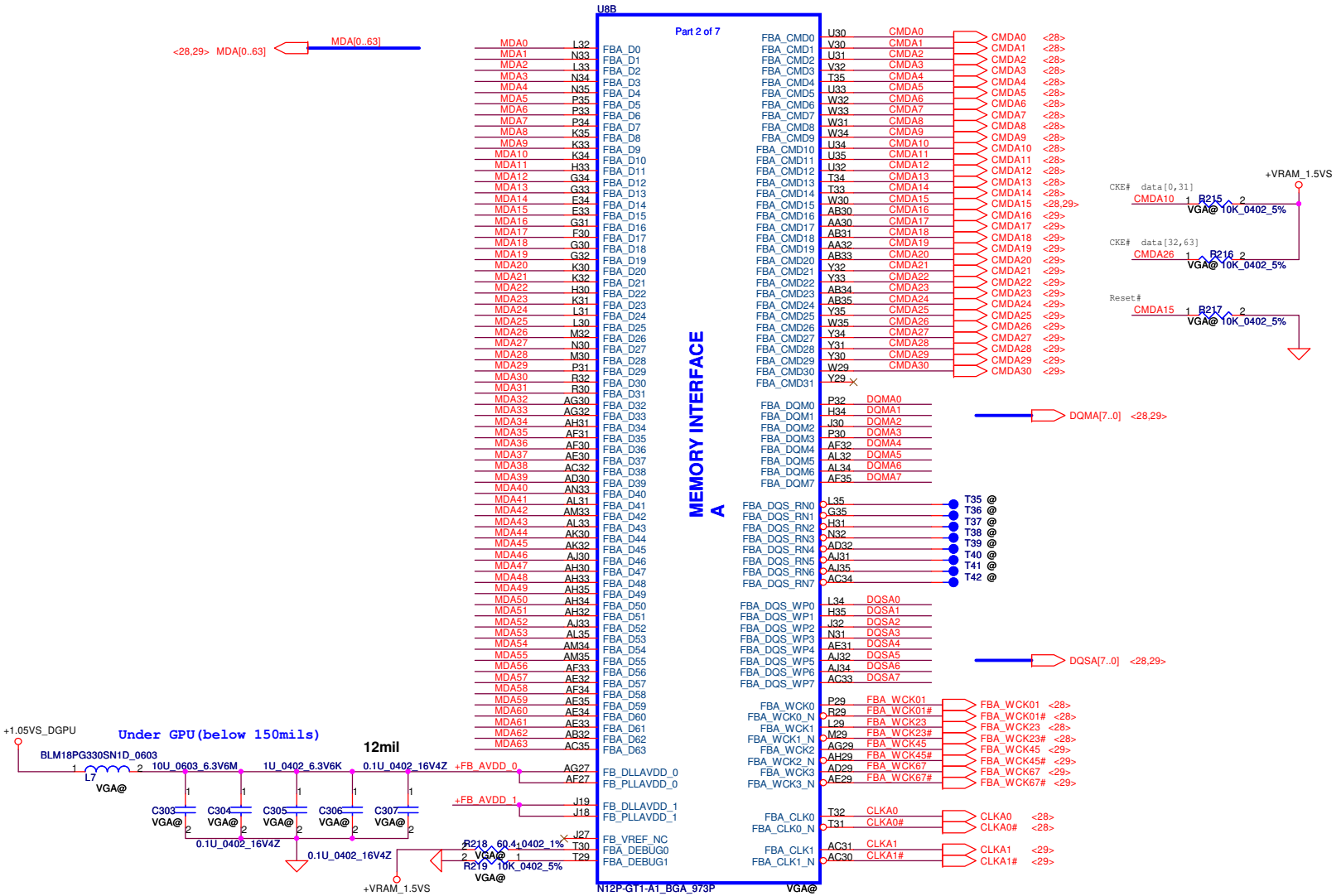
Compal Electronics, Inc.

Title: VGA(5/12)-GND

Size | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

Date: Thursday, November 04, 2010 | Sheet 25 of 62



Mode G- Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	A4_BA2	
CMD8	ABI#	
CMD2	A2_BA0	
CMD7	A6_A11	
CMD15	RESET#	
CMD13	RAS#	
CMD4	A5_BA1	
CMD6	A7_A8	
CMD12	A0_A10	
CMD10	CKE#	
CMD9	A12_RFU	
CMD1	A3_BA3	
CMD11	A1_A9	
CMD0	CS#	
CMD5	WE#	
CMD14	CAS#	
CMD30		RAS#
CMD20		A3_BA3
CMD16		WE#
CMD25		A12_RFU
CMD28		A7_A8
CMD22		A0_A10
CMD19		A2_BA0
CMD17		A5_BA1
CMD27		A6_A11
CMD29		CAS#
CMD18		A4_BA2
CMD15		RESET#
CMD26		CKE#
CMD23		A1_A9
CMD24		ABI#
CMD21		CS#

Security Classification	Compal Secret Data		
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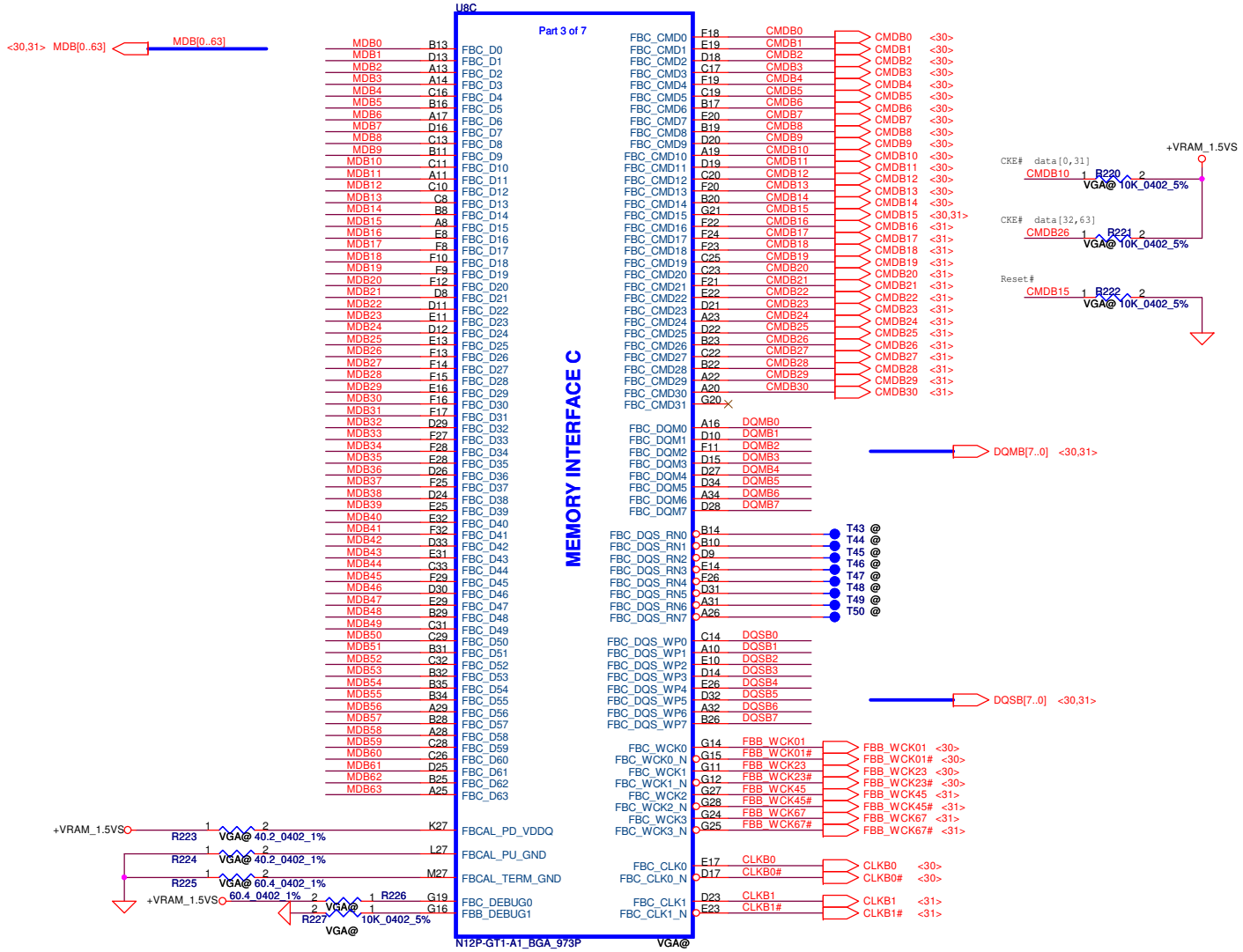
Compal Electronics, Inc.

Title: VGA(6/12)-MEM Interface A

Size | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

Date: Friday, November 05, 2010 | Sheet 26 of 62



Mode G- Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	A4_BA2	
CMD8	ABI#	
CMD2	A2_BA0	
CMD7	A6_A11	
CMD15	RESET#	
CMD13	RAS#	
CMD4	A5_BA1	
CMD6	A7_A8	
CMD12	A0_A10	
CMD10	CKE#	
CMD9	A12_RFU	
CMD1	A3_BA3	
CMD11	A1_A9	
CMD0	CS#	
CMD5	WE#	
CMD14	CAS#	
CMD30		RAS#
CMD20		A3_BA3
CMD16		WE#
CMD25		A12_RFU
CMD28		A7_A8
CMD22		A0_A10
CMD19		A2_BA0
CMD17		A5_BA1
CMD27		A6_A11
CMD29		CAS#
CMD18		A4_BA2
CMD15		RESET#
CMD26		CKE#
CMD23		A1_A9
CMD24		ABI#
CMD21		CS#

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Compal Electronics, Inc.

Title: VGA(7/12)-MEM Interface C

Size | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

Date: Friday, November 05, 2010 | Sheet 27 of 62

MF=0
Byte 0 and 2

MF=1
Byte 1 and 3

U10

U11

170-BALL
SGRAM GDDR5

H5GQ1H24AFR-T2L_BGA170

X76_HYN@

+VRAM_1.5VS

MDA[0..63] <26,29>
DQMA[7..0] <26,29>
DQSA[7..0] <26,29>

+FBA_VREFC
+FBA_VREFD

R228 549_0402_1% VGA@
R229 549_0402_1% VGA@
R230 1.33K_0402_1% VGA@
R231 1.33K_0402_1% VGA@
R232 931_0402_1% VGA@
R233 931_0402_1% VGA@
C313 0.01U_0402_25V7K VGA@
C314 0.01U_0402_25V7K VGA@

<22,29,30,31> MEM_VREF

Q5 SSM3K7002FU_SC70-3 VGA@

R234 1K_0402_5% VGA@
R235 1K_0402_5% VGA@
R236 121_0402_1% VGA@
R237 121_0402_1% VGA@
C315 0.01U_0402_25V7K VGA@

R238 40.2_0402_1% VGA@
R239 160_0402_1% @
R240 40.2_0402_1% VGA@
C316 0.01U_0402_25V7K VGA@
CLKA0
CLKA0#
CLKA_R

10U_0603_6.3V6M
C317 VGA@
C318 VGA@
C319 VGA@

0.1U_0402_16V4Z
C320 VGA@
C321 VGA@
C322 VGA@
C323 VGA@
C324 VGA@
C325 VGA@

1U_0402_6.3V4Z
C326 VGA@
C327 VGA@
C328 VGA@
C329 VGA@
C330 VGA@
C331 VGA@
C332 VGA@
C333 VGA@

C742 330U_6.3V_M_R14 @
C1017 330U_6.3V_M @

10/23 Change symbol of C742 from SGA20331E10 to SF000002M00
11/2 Change PN of C742 from SF000002M00 to SF000001G00

9/7 Add

U10	U11
K4G10325FE-HC04 X76_SAM@	K4G10325FE-HC04 X76_SAM@
K4G20325FC-HC04 X76_SAM2G@	K4G20325FC-HC04 X76_SAM2G@
H5GQ2H24MFR-T2C X76_HYN2G@	H5GQ2H24MFR-T2C X76_HYN2G@

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Compal Electronics, Inc.

Title: VRAM_GDDR5 / Channel A

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

Date: Friday, November 05, 2010 | Sheet 28 of 62

MF=0
Byte 0 and 2

MF=1
Byte 1 and 3

U12

U13

MDA[0..63] <26,28>
DQMA[7..0] <26,28>
DQSA[7..0] <26,28>

+VRAM_1.5VS

R241 549_0402_1% VGA@
R242 549_0402_1% VGA@
R243 1.33K_0402_1% VGA@
R244 1.33K_0402_1% VGA@
16mil +FBA_VREFD_U
16mil +FBA_VREFC_U
C334 0.01U_0402_25V7K VGA@
C335 0.01U_0402_25V7K VGA@
R247 VGA@ 931_0402_1%
R248 VGA@ 931_0402_1%
<22,28,30,31> MEM_VREF
Q6 SSM3K7002FU_SC70-3 VGA@

R251 40.2_0402_1% VGA@
R252 @ 160_0402_1%
R253 40.2_0402_1% VGA@
CLKA1
CLKA1#
C337 0.01U_0402_25V7K VGA@

10U_0603_6.3V6M
C338 VGA@
C339 VGA@
C340 VGA@

0.1U_0402_16V4Z
C341 VGA@
C342 VGA@
C343 VGA@
C344 VGA@
C345 VGA@
C346 VGA@

1U_0402_6.3V4Z
C347 VGA@
C348 VGA@
C349 VGA@
C350 VGA@
C351 VGA@
C352 VGA@
C353 VGA@
C354 VGA@

C336 0.01U_0402_25V7K VGA@

R245 1K_0402_1% VGA@
R249 121_0402_1% VGA@
R246 1K_0402_1% VGA@
R250 121_0402_1% VGA@

170-BALL
SGRAM GDDR5
H5GQ1H24AFR-T2L_BGA170
X76_HYN@

	U12	U13
K4G10325FE-HC04 X76_SAM@		
K4G20325FC-HC04 X76_SAM2G@		
H5GQ2H24MFR-T2C X76_HYN2G@		

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Compal Electronics, Inc.

Title: **VRAM_DDDR5 / Channel A**

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.3

Date: Friday, November 05, 2010 | Sheet 29 of 62

MF=0
Byte 0 and 2

MF=1
Byte 1 and 3

U14

U15

MDB[0..63] <27,31>
DQMB[7..0] <27,31>
DQSB[7..0] <27,31>

+VRAM_1.5VS

+FBB_VREFD

+FBB_VREFC

MEM_VREF <22,28,29,31>

Q7
SSM3K7002FU_SC70-3
VGA@

CLKB0

CLKB0_R

+VRAM_1.5VS

10U_0603_6.3V6M

0.1U_0402_16V4Z

1U_0402_6.3V4Z

170-BALL
SGRAM GDDR5

H5GQ1H24AFR-T2L_BGA170

X76_HYN@

K4G10325FE-HC04
X76_SAM@

K4G10325FE-HC04
X76_SAM@

K4G20325FC-HC04
X76_SAM2G@

K4G20325FC-HC04
X76_SAM2G@

H5GQ2H24MFR-T2C
X76_HYN2G@

H5GQ2H24MFR-T2C
X76_HYN2G@

10/23 Change symbol of C743 from SGA20331E10 to SF000002M00
11/2 Change PN of C743 from SF000002M00 to SF000001G00

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Compal Electronics, Inc.

Title: **VRAM_GDDR5 / Channel B**

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.3

Date: Friday, November 05, 2010 | Sheet 30 of 62

MF=0
Byte 0 and 2

MF=1
Byte 1 and 3

U16

U17

MDB[0..63] <27,30>

DQMB[7..0] <27,30>

DQSB[7..0] <27,30>

+VRAM_1.5VS

R267 549_0402_1% VGA@

R268 549_0402_1% VGA@

16mil +FBB_VREFD_U

16mil +FBB_VREFC_U

R269 1.33K_0402_1% VGA@

C376 0.01U_0402_25V7K VGA@

R270 1.33K_0402_1% VGA@

C377 0.01U_0402_25V7K VGA@

R275 VGA@ 931_0402_1%

R276 VGA@ 931_0402_1%

<22,28,29,30> MEM_VREF

Q8 SSM3K7002FU_SC70-3 VGA@

R277 40.2_0402_1% VGA@

R278 @ 160_0402_1%

CLKB1

CLKB1#

R279 40.2_0402_1% VGA@

C379 0.01U_0402_25V7K VGA@

10U_0603_6.3V6M

C380 VGA@

C381 VGA@

C382 VGA@

C383 0.1U_0402_16V4Z VGA@

C384 VGA@

C385 VGA@

C386 VGA@

C387 VGA@

C388 VGA@

C389 1U_0402_6.3V4Z VGA@

C390 VGA@

C391 VGA@

C392 VGA@

C393 VGA@

C394 VGA@

C395 VGA@

C396 VGA@

10/22 Add C522~C525

C522 @ 0.1U_0402_16V4Z

C523 @

C524 @

C525 @ 0.1U_0402_16V4Z

C378 0.01U_0402_25V7K VGA@

R271 1K_0402_1% VGA@

R273 121_0402_1% VGA@

R272 1K_0402_1% VGA@

R274 121_0402_1% VGA@

170-BALL SGRAM GDDR5

H5GQ1H24AFR-T2L_BGA170

X76_HYN@

K4G10325FE-HC04 X76_SAM@

K4G20325FC-HC04 X76_SAM2G@

H5GQ2H24MFR-T2C X76_HYN2G@

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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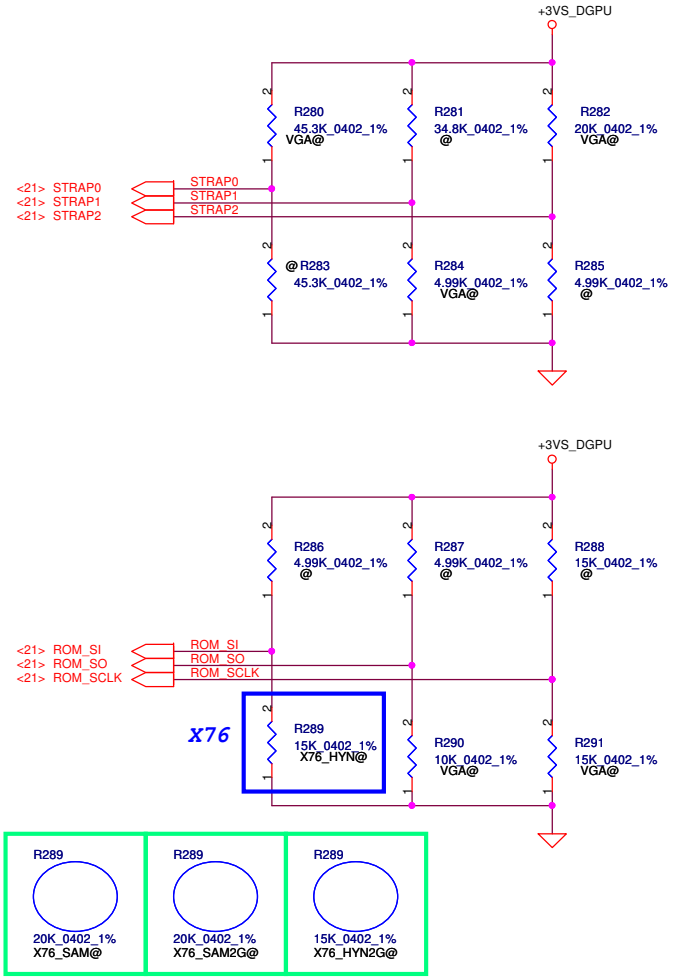
Compal Electronics, Inc.

Title: **VRAM_DDDR5 / Channel B**

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

Date: Friday, November 05, 2010 | Sheet 31 of 62



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Hynix H5GQ1H24AFR-T2L SA00003WL00	1G	0010	PD 15K
Samsung K4G10325FE-HC04 SA00003RS00	1G	0011	PD 20K

SUB_VENDOR

0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417

0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE

0	256MB (Default)
1	Reserved

USER Straps

User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG

3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM

0	Disable (Default)
1	Enable

SLOT_CLK_CFG

0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE

0	3D Device
1	VGA Device (Default)

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Issued Date	2010/07/20	Deciphered Date	2011/07/20

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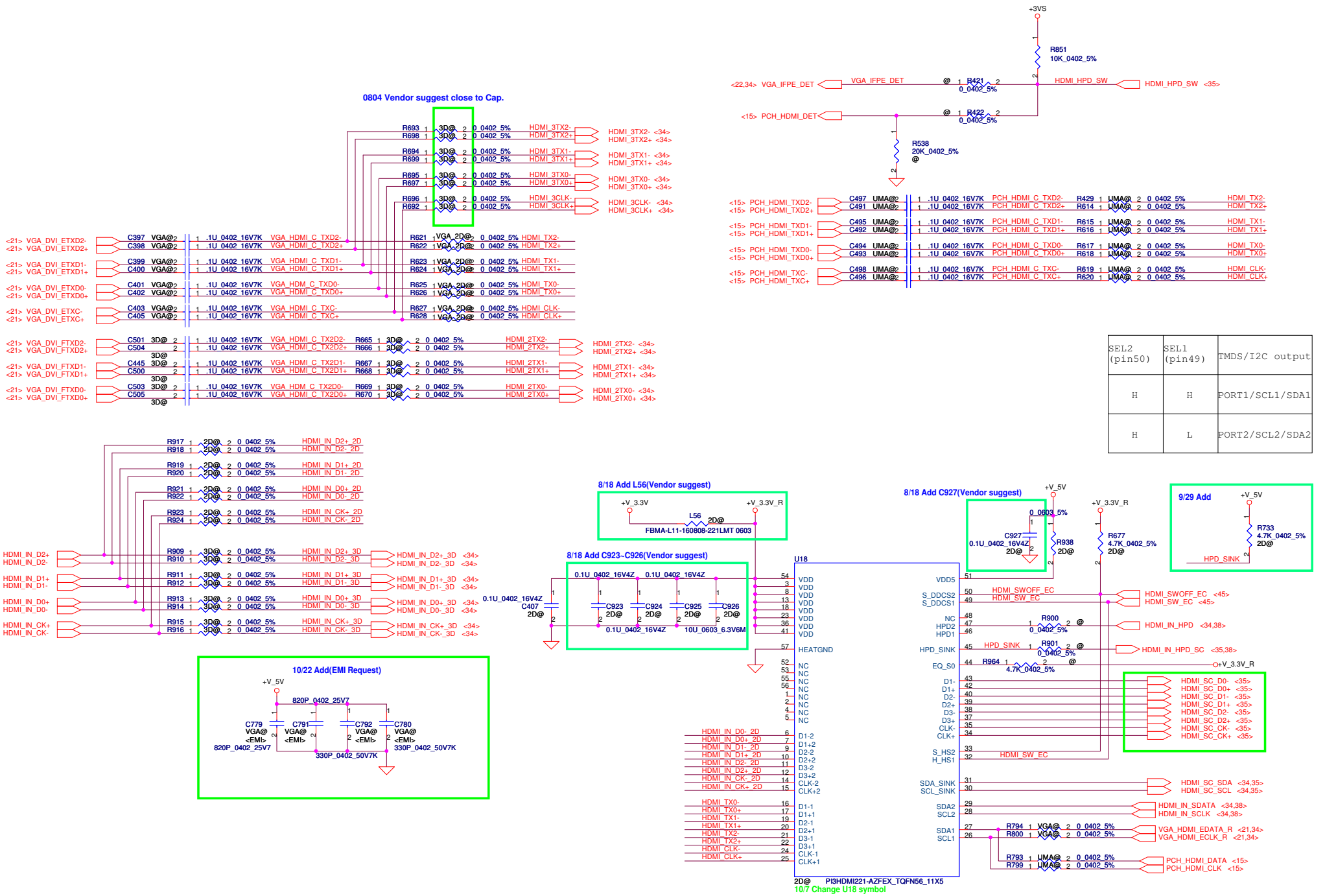
Compal Electronics, Inc.
Title: VGA(12/12)-MISC
Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3
Date: Friday, November 05, 2010 | Sheet 32 of 62



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Issued Date	2010/07/20	Deciphered Date 2011/07/20

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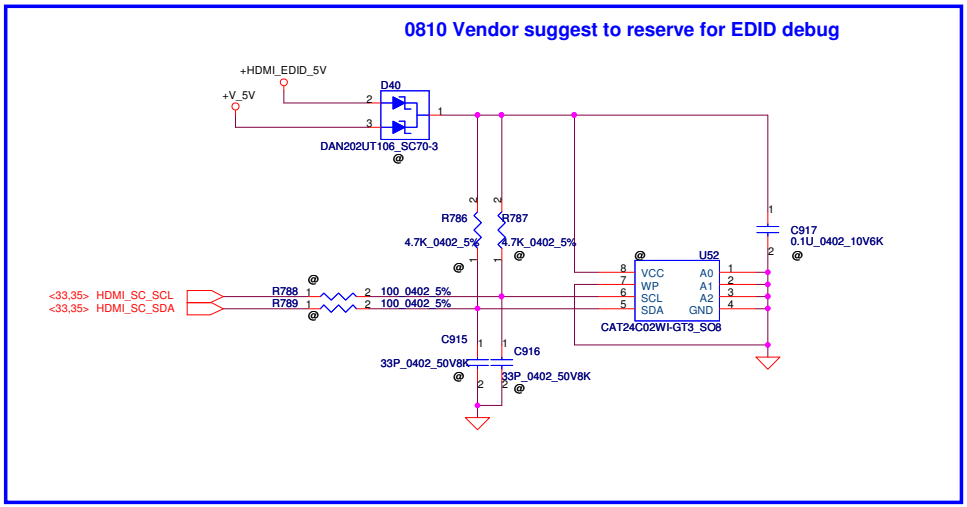
Compal Electronics, Inc.

Title: HDMI Switch

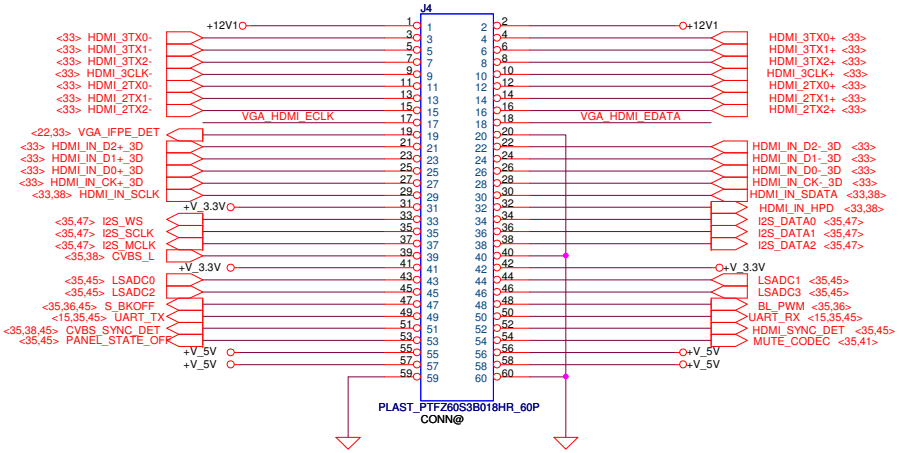
Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

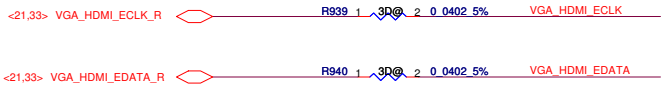
Date: Friday, November 05, 2010 | Sheet 33 of 62

0810 Vendor suggest to reserve for EDID debug



1003 IO/B Pin define update





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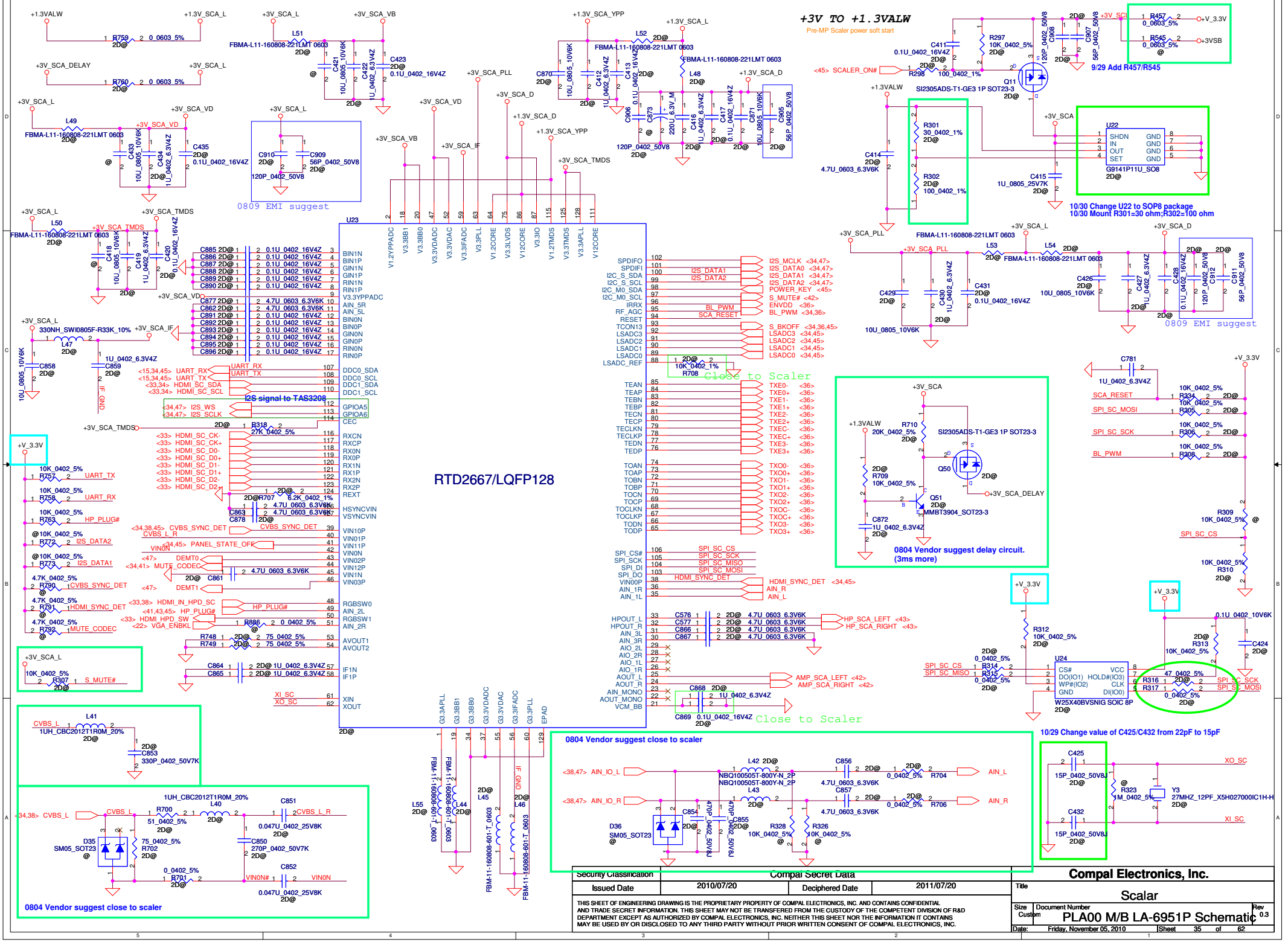
Compal Electronics, Inc.

Title: 3D Scalar

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

Date: Friday, November 05, 2010 | Sheet 34 of 62


+3V TO +1.3VALW
Pre-MP Scaler power soft start
9/29 Add R457/R545
10/30 Change U22 to SOP8 package
10/30 Mount R301=30 ohm;R302=100 ohm
0809 EMI suggest
RTD2667/LQFP128
I2S signal to TAS3208
Close to Scaler
0804 Vendor suggest delay circuit.
(3ms more)
10/29 Change value of C425/C432 from 22pF to 15pF
0804 Vendor suggest close to scaler
Compal Electronics, Inc.
Scalar
PLA00 M/B LA-6951P Schematic
Rev 0.3
Security Classification: Compal Secret Data
Issued Date: 2010/07/20
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Date: Friday, November 05, 2010
Sheet 35 of 62

WebCam+Digital Mic

5/18 Change R332 from 100K to 10K ohm

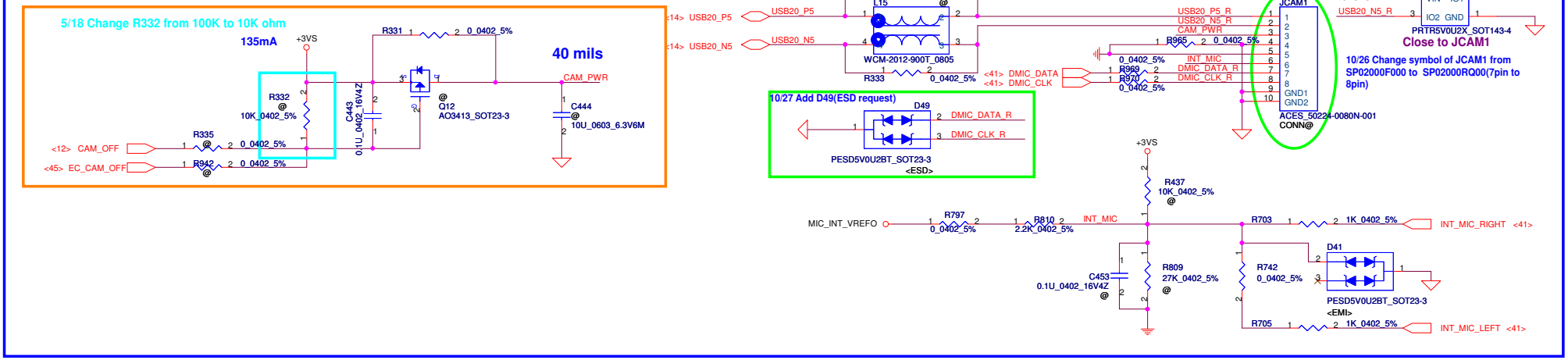
135mA

40 mils

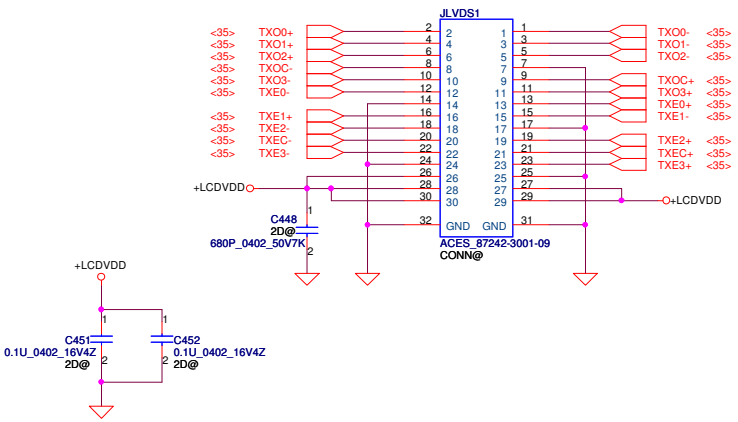
10/26 Change symbol of JCAM1 from SP02000F000 to SP02000RQ00(7pin to 8pin)

Close to JCAM1

10/27 Add D49(ESD request)



LVDS CONN

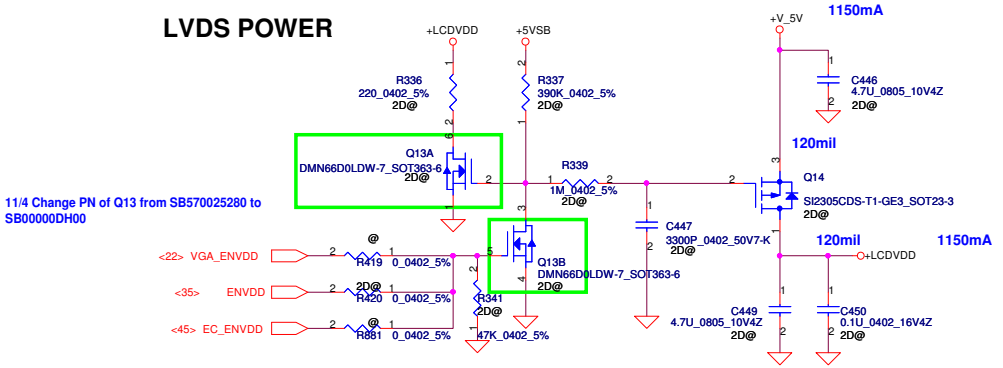


LVDS POWER

11/4 Change PN of Q13 from SB570025280 to SB00000DH00

1150mA

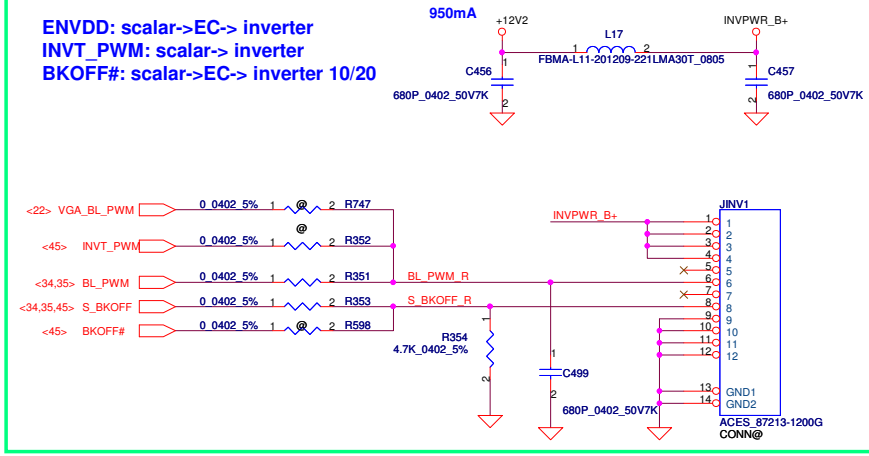
120mil



INVERTER

ENVDD: scalar->EC-> inverter
INVT_PWM: scalar-> inverter
BKOFF#: scalar->EC-> inverter 10/20

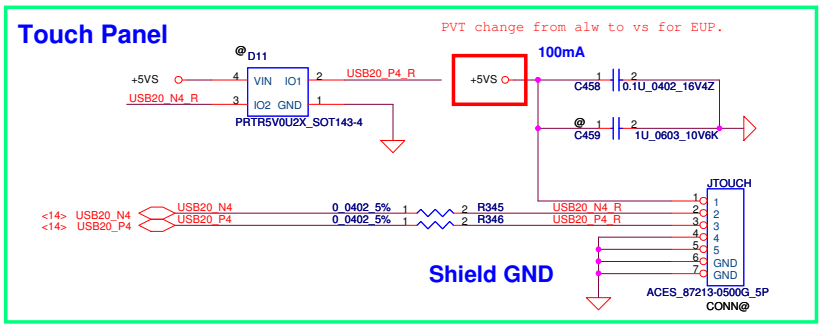
950mA



Touch Panel

PVT change from alw to vs for EUP.

100mA



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Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Compal Electronics, Inc.

Title: LCD CONN. / WebCam

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.3

Date: Friday, November 05, 2010 | Sheet 36 of 62

HDD POWER Conn

+12VS 8/18 Add C918~C921

C920 0.1U_0402_16V4Z
C918 10U_0805_25V_K
C921 0.1U_0402_16V4Z
C919 10U_0805_10V4Z

Layout Note:Place C918/C919/C920/C921 close to JWAFER1

HDD

JWAF1
ACES_50310-00671-001_6P
CONN@

10/28 Change footprint of JWAFER1 from LTCX002XR00 to LTCX0033X00

SATA HDD Conn.

JHDD1
LOTES_ABA-SAT-049-K
CONN@

ODD POWER Conn

+12VS 10/29 Add C930/C931

C930 0.1U_0402_16V4Z
C931 10U_0805_25V_K
C928 0.1U_0402_16V4Z
C929 10U_0805_10V4Z

10/28 Add C928/C929

Layout Note:Place C928/C929 close to JWAFER2

JWAF2
ACES_50310-00671-001_6P
CONN@

10/28 Add footprint of JWAFER2 to LTCX0033X00

ODD

SATA ODD Conn.

JODD1
LOTES_ABA-SAT-049-K
CONN@

SSD

MINI SSD Conn.

JMINI3
BELLW_80003-1021
CONN@

SATA SSD Conn.

JSSD1
LOTES_ABA-SAT-049-K
CONN@

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Compal Electronics, Inc.

Title: HDD & ODD & SSD Connector

Size: B | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

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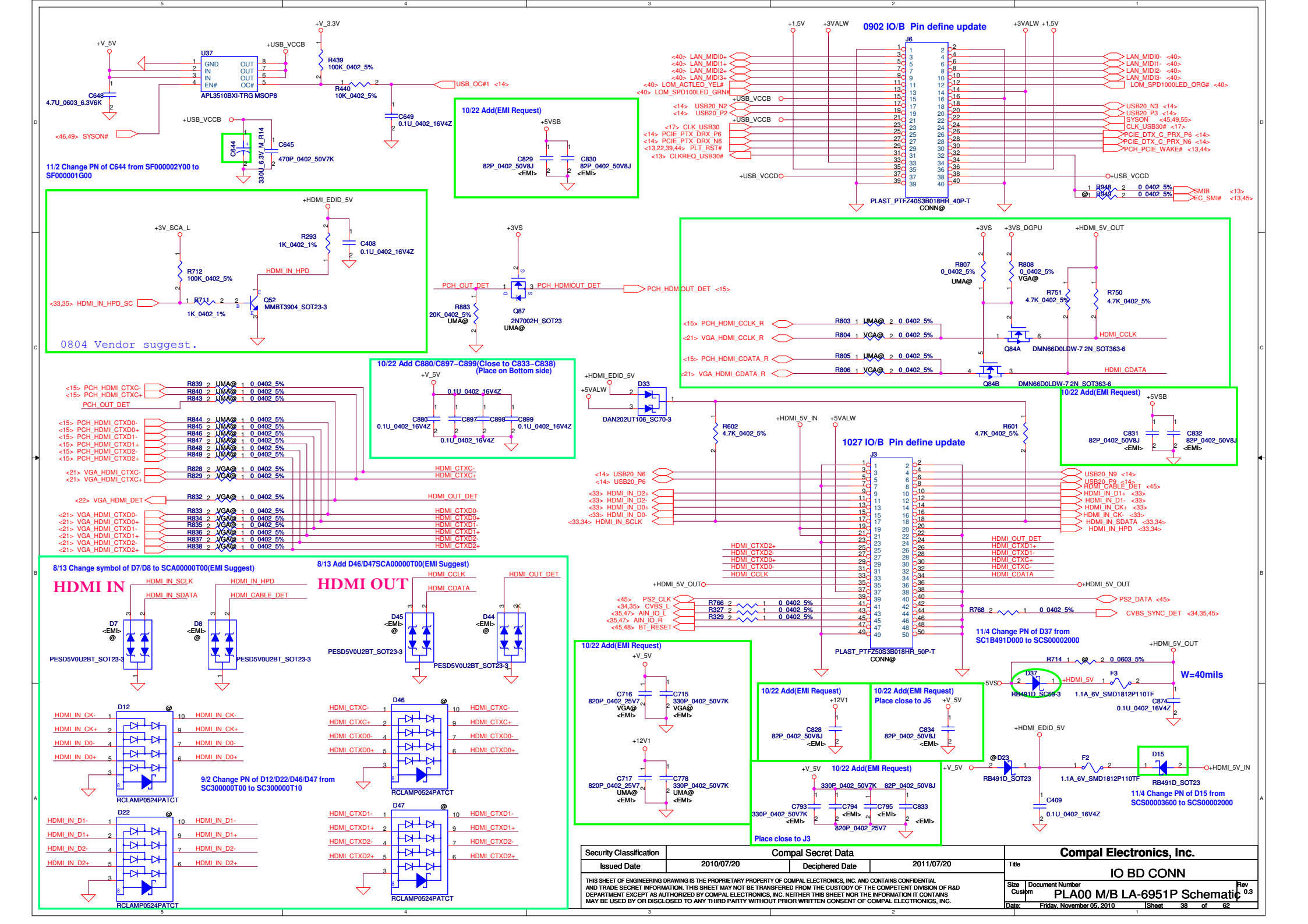
0902 IO/B Pin define update
1027 IO/B Pin define update
0804 Vendor suggest.
11/2 Change PN of C644 from SF000002Y00 to SF000001G00
10/22 Add(EMI Request)
10/22 Add C880/C897~C899(Close to C833~C838) (Place on Bottom side)
8/13 Change symbol of D7/D8 to SCA00000T00(EMI Suggest)
8/13 Add D46/D47SCA00000T00(EMI Suggest)
HDMI IN
HDMI OUT
9/2 Change PN of D12/D22/D46/D47 from SC300000T00 to SC300000T10
11/4 Change PN of D37 from SC1B491D000 to SCS00002000
11/4 Change PN of D15 from SCS00003600 to SCS00002000
W=40mils
Place close to J3
Place close to J6
Security Classification
Compal Secret Data
Issued Date
2010/07/20
Deciphered Date
2011/07/20
Compal Electronics, Inc.
IO BD CONN
PLA00 M/B LA-6951P Schematic
Rev 0.3
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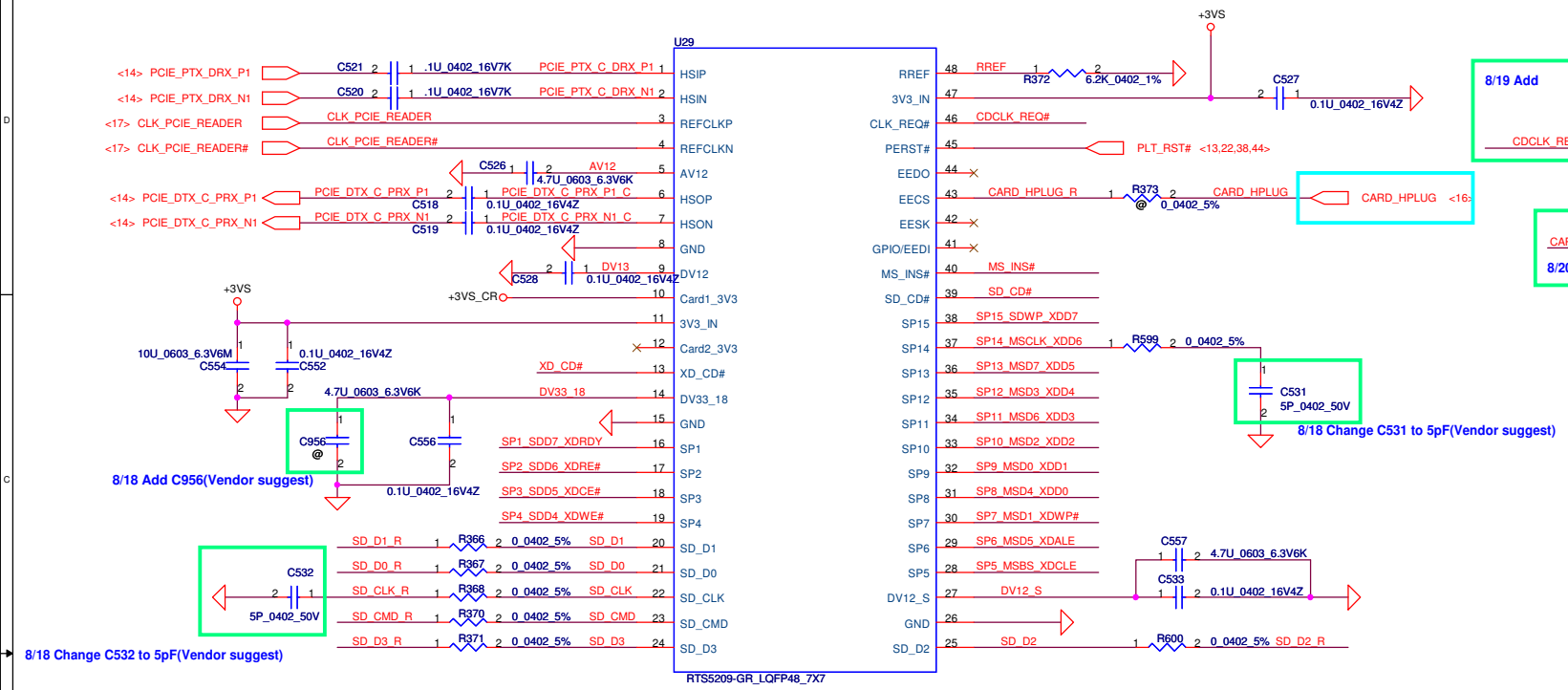
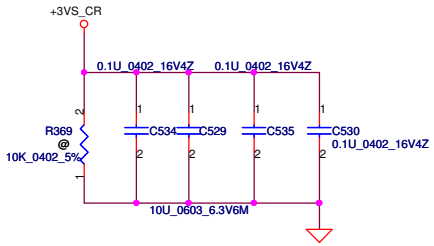




Place C534 close to socket pin 38

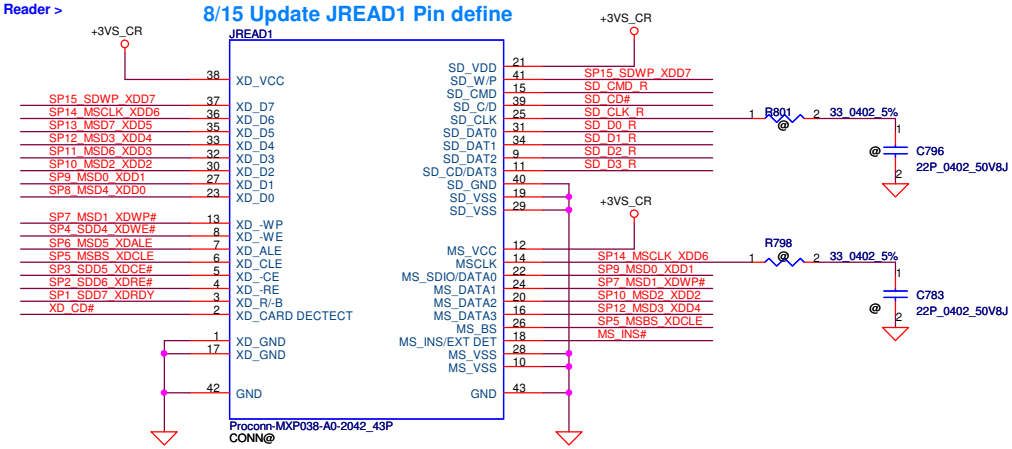
Place C529 close to socket pin 21

Place C535 close to socket pin 21

Place C530 close to socket pin 12

< 7 in 1 Card Reader >

8/15 Update JREAD1 Pin define



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Compal Electronics, Inc.

Title: PCIE-Card Reader-RTS5209

Size | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

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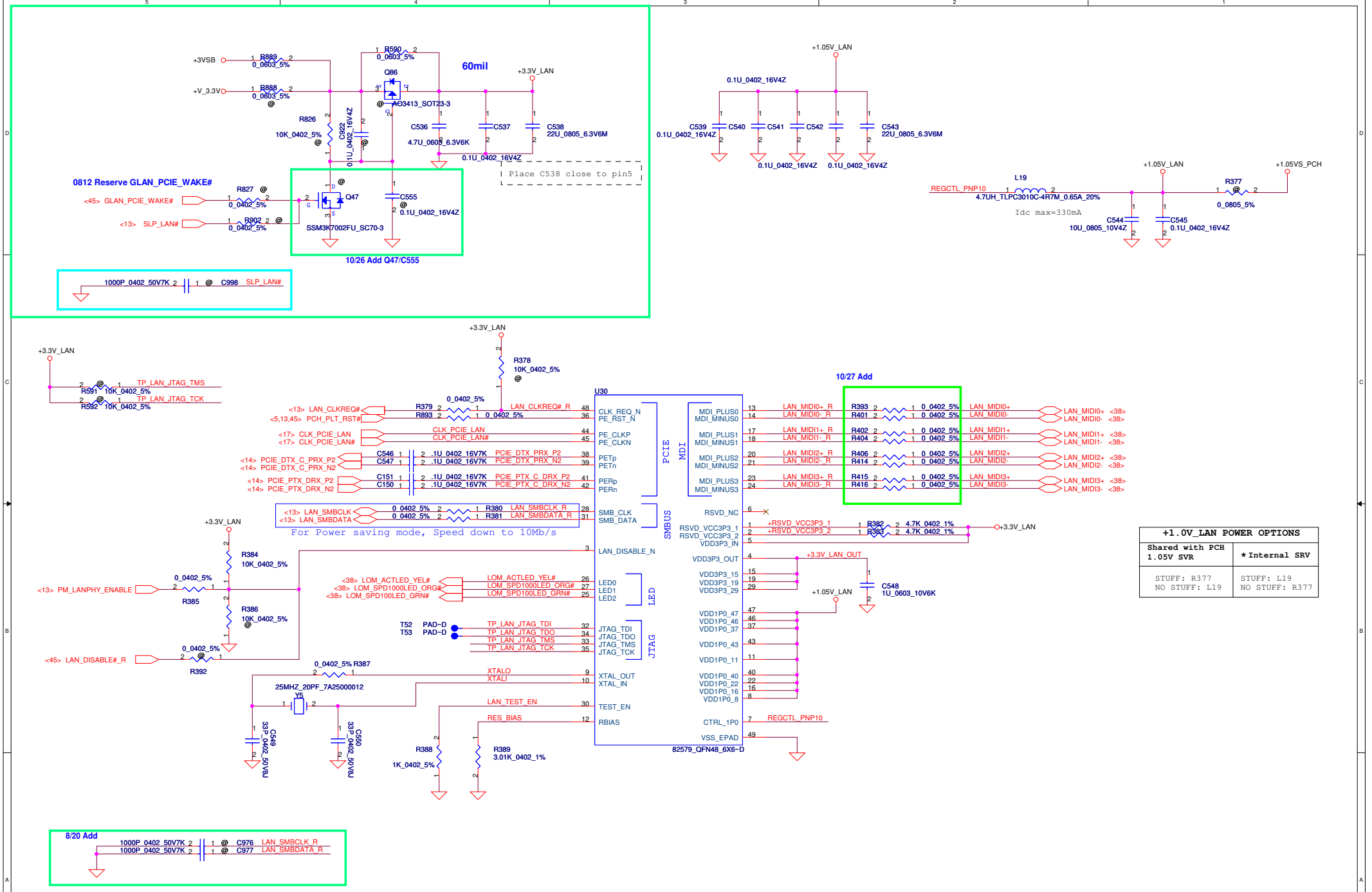

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Compal Electronics, Inc.

Title: Intel LAN-82579

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

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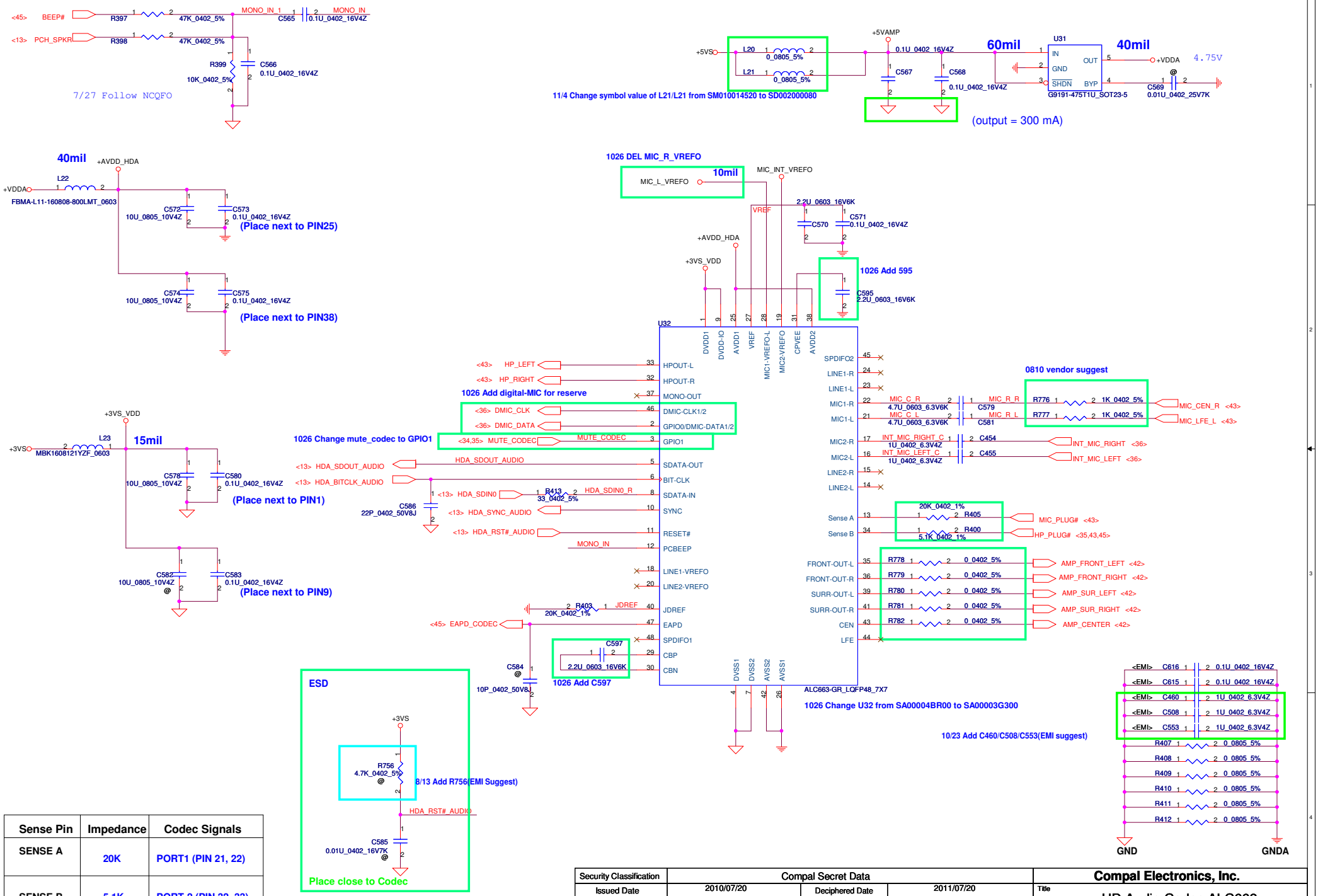

Sense Pin	Impedance	Codec Signals
SENSE A	20K	PORT1 (PIN 21, 22)
SENSE B	5.1K	PORT-2 (PIN 32, 33)

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: HD Audio Codec ALC663

Size	Document Number	Rev
B	PIA00 M/B LA-6951P Schematic	0.3

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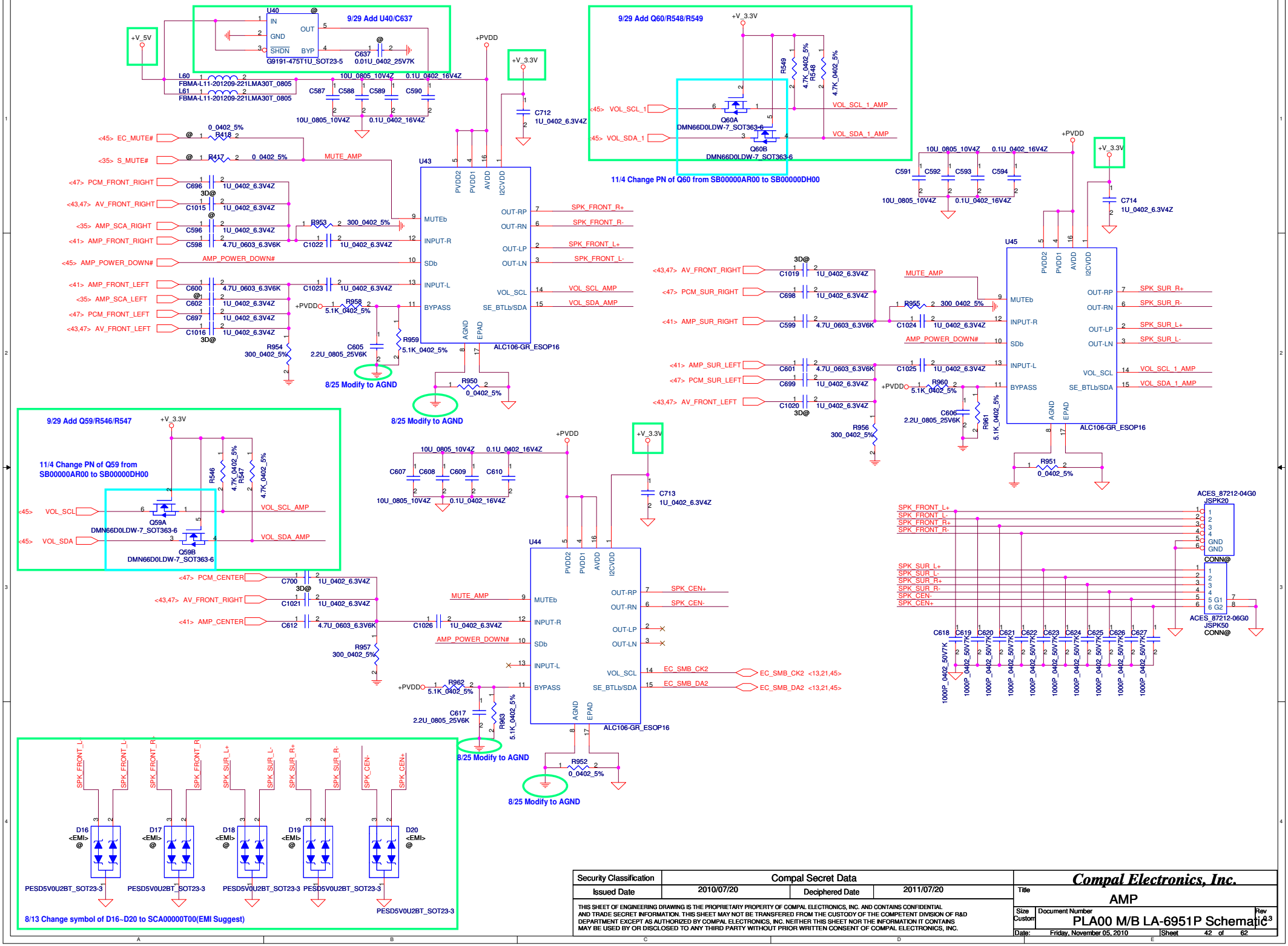

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Compal Electronics, Inc.

Title: AMP

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.3

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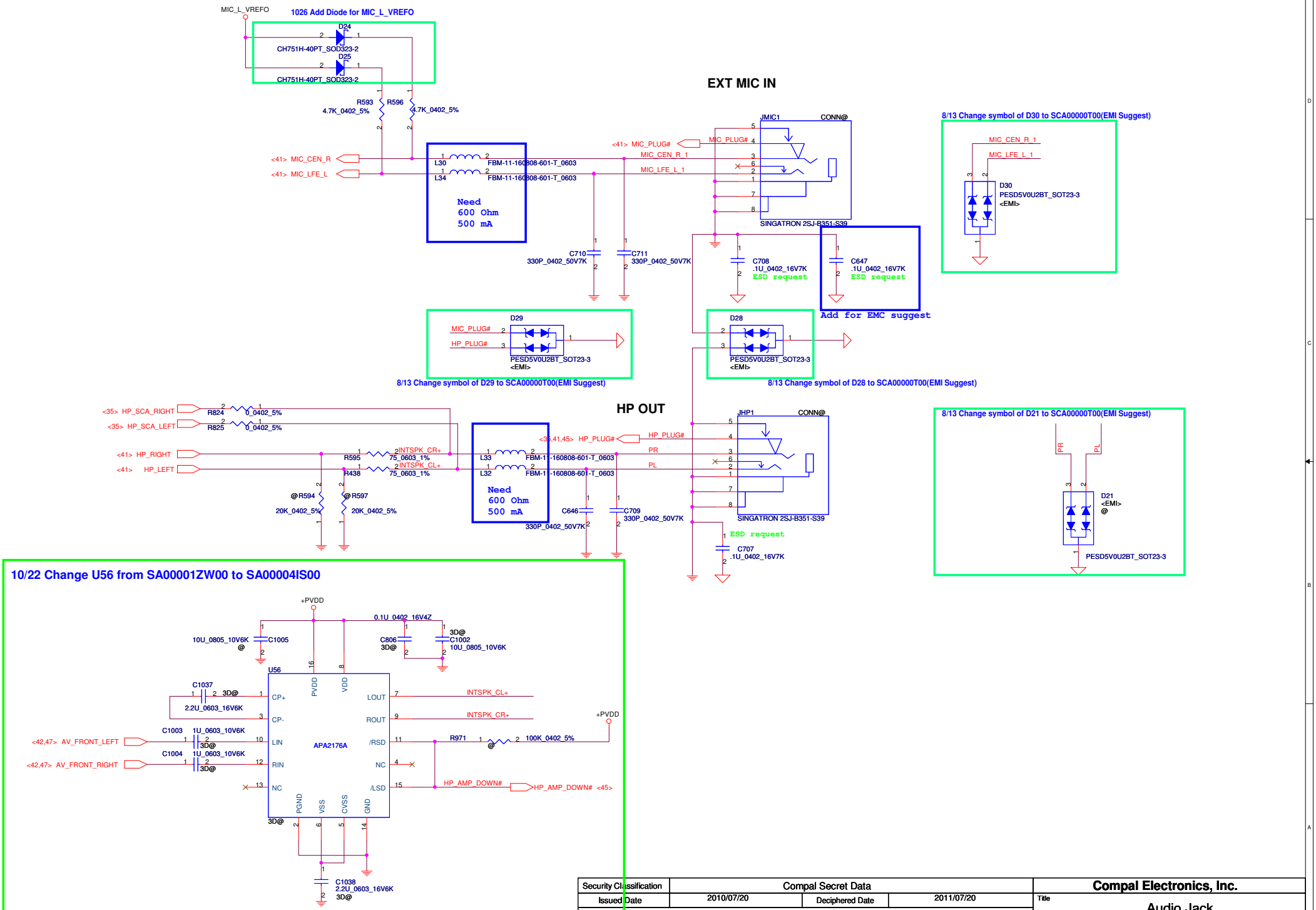
MIC_L_VREFO
1026 Add Diode for MIC_L_VREFO
D24
CH751H-40PT_SOD323-2
D25
CH751H-40PT_SOD323-2
R593
4.7K_0402_5%
R596
4.7K_0402_5%
EXT MIC IN
<41> MIC_CEN_R
<41> MIC_LFE_L
L30
FBM-11-160808-601-T_0603
L34
FBM-11-160808-601-T_0603
Need
600 Ohm
500 mA
<41> MIC_PLUG#
MIC_PLUG#
MIC_CEN_R_1
MIC_LFE_L_1
JMIC1
CONN@
SINGATRON 2SJ-B351-S39
C710
330P_0402_50V7K
C711
330P_0402_50V7K
C708
.1U_0402_16V7K
ESD request
C647
.1U_0402_16V7K
ESD request
Add for EMC suggest
8/13 Change symbol of D30 to SCA00000T00(EMI Suggest)
MIC_CEN_R_1
MIC_LFE_L_1
D30
PESD5V0U2BT_SOT23-3
<EMI>
D29
MIC_PLUG#
HP_PLUG#
PESD5V0U2BT_SOT23-3
<EMI>
8/13 Change symbol of D29 to SCA00000T00(EMI Suggest)
D28
PESD5V0U2BT_SOT23-3
<EMI>
8/13 Change symbol of D28 to SCA00000T00(EMI Suggest)
HP OUT
<35> HP_SCA_RIGHT
<35> HP_SCA_LEFT
R824
0_0402_5%
R825
0_0402_5%
<41> HP_RIGHT
<41> HP_LEFT
R595
75_0603_1%
R438
75_0603_1%
INTSPK_CR+
INTSPK_CL+
@R594
20K_0402_5%
@R597
20K_0402_5%
L33
FBM-11-160808-601-T_0603
L32
FBM-11-160808-601-T_0603
Need
600 Ohm
500 mA
<34,41,45> HP_PLUG#
HP_PLUG#
PR
PL
JHP1
CONN@
SINGATRON 2SJ-B351-S39
C646
330P_0402_50V7K
C709
330P_0402_50V7K
ESD request
C707
.1U_0402_16V7K
8/13 Change symbol of D21 to SCA00000T00(EMI Suggest)
PR
PL
D21
<EMI>
@
PESD5V0U2BT_SOT23-3
10/22 Change U56 from SA00001ZW00 to SA00004IS00
+PVDD
0.1U_0402_16V4Z
10U_0805_10V6K
@
C1005
C806
3D@
3D@
C1002
10U_0805_10V6K
U56
APA2176A
PVDD
VDD
CP+
CP-
LIN
RIN
NC
LOUT
ROUT
/RSD
NC
/LSD
PGND
VSS
CVSS
GND
C1037
3D@
2.2U_0603_16V6K
C1003
1U_0603_10V6K
3D@
C1004
1U_0603_10V6K
3D@
<42,47> AV_FRONT_LEFT
<42,47> AV_FRONT_RIGHT
INTSPK_CL+
INTSPK_CR+
R971
@
100K_0402_5%
HP_AMP_DOWN#
HP_AMP_DOWN# <45>
C1038
2.2U_0603_16V6K
3D@
Security Classification
Compal Secret Data
Issued Date
2010/07/20
Deciphered Date
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Compal Electronics, Inc.
Title
Audio Jack
Size
Custom
Document Number
PLA00 M/B LA-6951P Schematic
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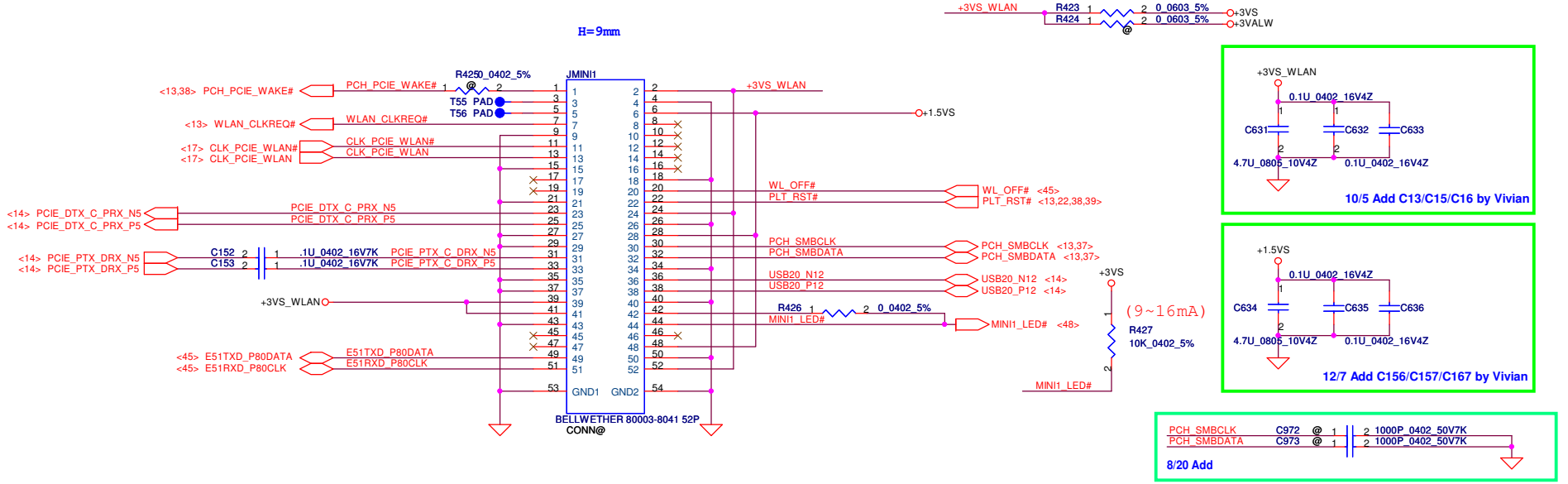
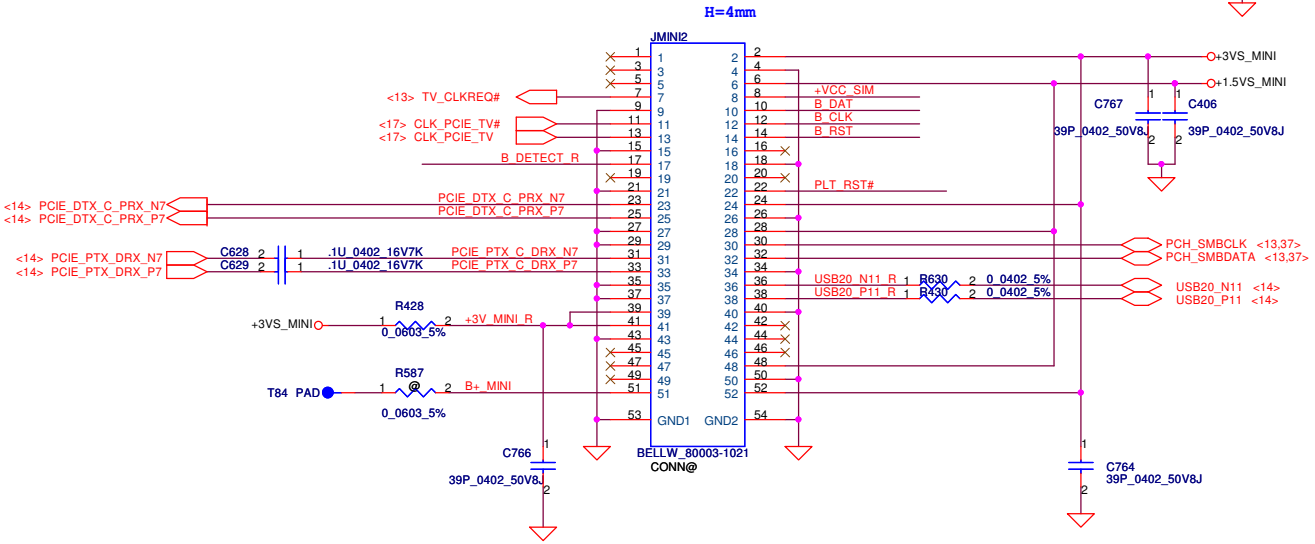
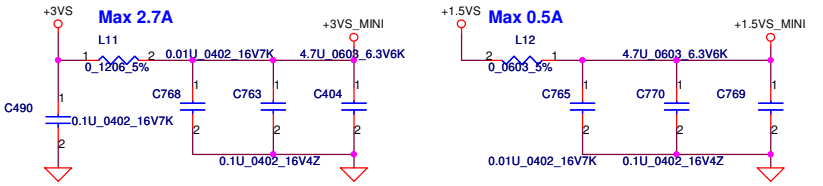
WLAN

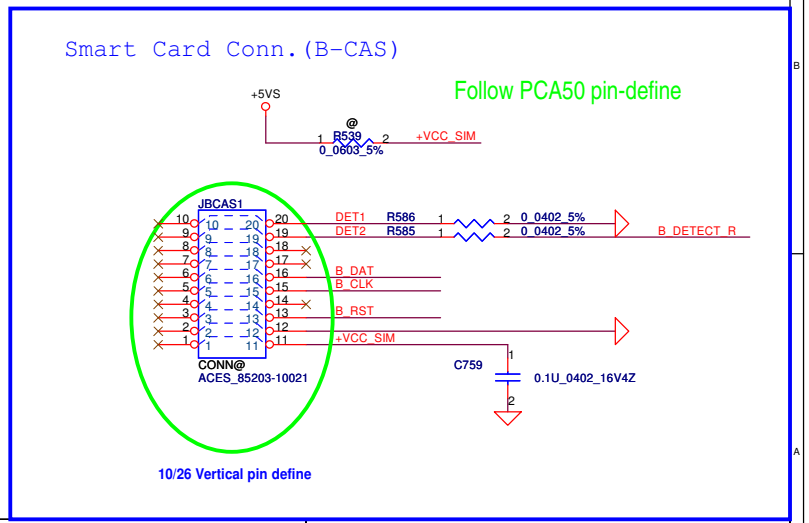


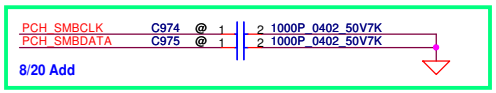
MINI

Mini Card Slot 1---TV tuner Currecnt: 3.3 : 2750mA, 1.5: 500mA









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Compal Electronics, Inc.

Title: **WLAN&MINI**

Size: Custom | Document Number: **PLA00 M/B LA-6951P Schematic** | Rev: 0.3

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Place closely pin 12

CLK_PCI_LPC — R444 10_0402_5% — C657 18P_0402_50V8J

Place closely pin 13

PCH_PLT_RST# — @ C658 0.1U_0402_16V4Z

1000P_0402_50V7K C650 — 0.1U_0402_16V4Z C651 C652 — 0.1U_0402_16V4Z C653 C654 — 0.1U_0402_16V4Z C655

+3VSB — R552 0_0603_5% — R441 0_0603_5%

+EC_AVCC — C656 0.1U_0402_16V4Z — ECAGND — R443 @ 0_0402_5%

VR_HOT# <57> — R447 0_0402_5% — H_PROCHOT# <5>

H_PROCHOT#_EC — Q42 2N7002H_SOT23 — C860 47P_0402_50V8J

U46 — KB930QF-A1_LQFP128_14X14

GATEA20/GPIO00 — EC_GA20 <12>
KBRST#/GPIO01 — EC_KBRST# <12>
SERIRQ# — SERIRQ <12>
LPC_FRAME#/LFRAME# — LPC_FRAME# <13>
LPC_AD3/LAD3 — LPC_AD3 <13>
LPC_AD2/LAD2 — LPC_AD2 <13>
LPC_AD1/LAD1 — LPC_AD1 <13>
LPC_AD0/LAD0 — LPC_AD0 <13>
LPC & MISC

CLK_PCI_EC/PCICLK — CLK_PCI_LPC <17>
PCIRST#/GPIO05 — PCH_PLT_RST# <5,13,40>
EC_RST#/ECRST# — ECRST#
EC_SCI#/GPIO0E — EC_SCI# <12>
CLKRUN#/GPIO1D — CLKRUN# <13>

+3VSB — R446 47K_0402_5% — C659 0.1U_0402_16V4Z — R925 @ 0_0402_5%

PWM Output
PWM0/GPIO0F — EC_OSD_PWM — EC_OSD_PWM <48>
BEEP#/PWM1/GPIO10 — BEEP# <41>
FANPWM0/GPIO12 — FAN_CPU_PWM <48>
ACOFF/FANPWM1/GPIO13 — FAN_GPU_PWM <48>

AD Input
BATT_TEMP/AD0/GPI38 — GFXVR_IMON — GFXVR_IMON <57>
BATT_OVP/AD1/GPI39 — AD_BID
ADP_I/AD2/GPI3A — IMVP_IMON
AD3/GPI3B
AD4/GPI42
AD5/GPI43

+3VSB — Ra R442 100K_0402_5% — AD_BID — Rb R445 0_0603_5% @

DA Output
DAC_BRIG/DA0/GPO3C — R762 0_0402_5% — LSADC0 <34,35>
EN_DFAN1/DA1/GPO3D — R761 0_0402_5% — LSADC1 <34,35>
IREF/DA2/GPO3E — R449 0_0402_5% — LSADC2 <34,35>
DA3/GPO3F — R450 0_0402_5% — LSADC3 <34,35>

LSADC0 R492 100K_0402_5%
LSADC1 R493 100K_0402_5%
LSADC2 R494 100K_0402_5%
LSADC3 R495 100K_0402_5%
10/5 Add R492~495(EC request)

PS2 Interface
EC_MUTE#/PSCLK1/GPIO4A — PS2_CLK — PS2_CLK <38>
USB_EN#/PSDAT1/GPIO4B — PS2_DATA — PS2_DATA <38>
CAP_INT#/PSCLK2/GPIO4C — VOL_SCL_1 — VOL_SCL_1 <42>
PSDAT2/GPIO4D — VOL_SDA_1 — VOL_SDA_1 <42>
TP_CLK/PSCLK3/GPIO4E — EC_3V5V_EN — EC_3V5V_EN <52>
TP_DATA/PSDAT3/GPIO4F — HP_AMP_DOWN# — HP_AMP_DOWN# <43>

SPI Device I/F
SDICS#/GPXIOA00 — VGATE_R — R453 0_0402_5% — VGATE — VGATE <13,57>
WOL_EN/SDICLK/GPXIOA01 — LAN_DISABLE# — LAN_DISABLE#_R <40>
ME_EN/SDIMOSI/GPXIOA02 — ME_FLASH <13>
LID_SW#/GPXIOD00 — SCALER_ON# <35>

SPI Flash ROM
SPIDI/MISO — EC_SI_SPI_SO — EC_SI_SPI_SO <46>
SPIDO/MOSI — EC_SO_SPI_SI — EC_SO_SPI_SI <46>
SPICLK/GPIO58 — SPI_CLK — R454 33_0402_5% — SPI_CLK_R <46>
SPICS# — SPI_CS# — SPI_CS# <46>

GPIO
GPIO40 — CIR_IN — R455 10K_0402_5% — CIR_IN <48>
H_PECI/GPIO41 — H_PECI — H_PECI <5,12>
FSTCHG/GPIO50 — GLAN_PCIE_WAKE# — GLAN_PCIE_WAKE# <40>
BATT_CHG_LED#/GPIO52 — SSD_DET# <37>
CAPS_LED#/GPIO53 — BT_OFF# <48>
BATT_LOW_LED#/GPIO54 — WL_BLUE_LED# — WL_BLUE_LED# <48>
PWR_LED#/GPIO55 — PWR_ON_LED# — PWR_ON_LED# <48>
SYSON/GPIO56 — SYSON — SYSON <38,49,55>
VR_ON/XCLK32K/GPIO57 — VR_ON — VR_ON <57>
AC_IN/GPIO59

+3VSB — @ C660 100P_0402_50V8J

9/29 Change net name from +V_5V to +5VSB
+5VSB — PS2_CLK 4.7K_0402_5% @ R927 — PS2_DATA 4.7K_0402_5% @ R928

Int. K/B Matrix
KSI0/GPIO30 — UART_TX_R
KSI1/GPIO31 — EC_MUTE# — AMP_POWER_DOWN# — CVBS_SYNC_DET — HDMI_SYNC_DET — HP_PLUG# — BT_RESET
KSI2/GPIO32
KSI3/GPIO33
KSI4/GPIO34
KSI5/GPIO35
KSI6/GPIO36
KSI7/GPIO37 — J5 @ 10K_0603_5%
KSO0/GPIO20 — KSO1 — KSO2
KSO1/GPIO21
KSO2/GPIO22
KSO3/GPIO23
KSO4/GPIO24 — EC_OSD_RST# — SOURCE_LED — EC_CAM_OFF — AV_AUDIO_SEL# — HDMI_SW_EC — EC_ENVDD
KSO5/GPIO25 — HDMI_SWOFF_EC
KSO6/GPIO26 — J8 @ 10K_0603_5% — UART_RX_R — H_PROCHOT#_EC — EC_REVPWROK
KSO7/GPIO27
KSO8/GPIO28
KSO9/GPIO29
KSO10/GPIO2A
KSO11/GPIO2B
KSO12/GPIO2C
KSO13/GPIO2D
KSO14/GPIO2E
KSO15/GPIO2F
KSO16/GPIO48
KSO17/GPIO49

+3VSB — 4.7K_0402_5% R968 KSI7 — 10/25 Add R968

+3VSB — R451 47K_0402_5% KSO1 — R452 47K_0402_5% KSO2 — 8/15 Add

<15,34,35> UART_TX — R474 0_0402_5% — UART_TX_R
<15,34,35> UART_RX — R485 0_0402_5% — UART_RX_R

<34,35> PANEL_STATE_OFF — 1K_0402_1% R884 — 8/19 Add R884(Vendor suggest)

SM Bus
EC_SMB_CK1/SCL0/GPIO44 — VOL_SCL — VOL_SCL <42>
EC_SMB_DA1/SDA0/GPIO45 — VOL_SDA — VOL_SDA <42>
EC_SMB_CK2/SCL1/GPIO46 — EC_SMB_CK2_M — EC_SMB_CK2
EC_SMB_DA2/SDA1/GPIO47 — EC_SMB_DA2_M — EC_SMB_DA2

1000P_0402_50V7K C982 @ EC_SMB_CK2
1000P_0402_50V7K C983 @ EC_SMB_DA2
8/20 Add

EC DEBUG port
Reserve R460 for EC debug.
R460 E51TXD_P80DATA 100K_0603_5%

GPIO
PM_SLP_S3#/GPIO04 — PM_SLP_S3# — PM_SLP_S3 <13>
PM_SLP_S5#/GPIO07 — PM_SLP_S5# — PM_SLP_S5 <13>
EC_SMI#/GPIO08 — EC_SMI# — EC_SMI <13,38>
GPIO0A — EC_ESB_INT — EC_ESB_INT <48>
GPIO0B — EC_OSD_CK — EC_OSD_CK <48>
GPIO0C — EC_OSD_DA — EC_OSD_DA <48>
SUS_PWR_DN_ACK/GPIO0D — SUS_PWR_ACK — SUS_PWR_ACK <13>
INVT_PWM/PWM2/GPIO11 — INVT_PWM — INVT_PWM <36>
FAN_SPEED1/FANFB0/GPIO14 — FAN_CPU_SPEED — FAN_CPU_SPEED <48>
FANFB1/GPIO15 — FAN_GPU_SPEED — FAN_GPU_SPEED <48>
EC_TX/GPIO16 — E51TXD_P80DATA — E51TXD_P80DATA <44>
EC_RX/GPIO17 — E51RXD_P80CLK — E51RXD_P80CLK <44>
ON_OFF/GPIO18 — ON/OFF — ON/OFF <50>
SUSP_LED#/GPIO19 — CEN_PWR_LED — CEN_PWR_LED <48>
NUM_LED#/GPIO1A — SUSWARN# — SUSWARN# <13>

GPO
EC_RSMRST#/GPXIOA03 — EC_RSMRST# — EC_RSMRST# <13>
EC_LID_OUT#/GPXIOA04 — VCCSA_PG — VCCSA_PG <53>
EC_ON/GPXIOA05 — EC_ON <50>
EC_SWI#/GPXIOA06 — EC_SWI# <13>
ICH_PWROK/GPXIOA07 — EC_PWROK — EC_PWROK <13>
BKOFF#/GPXIOA08 — BKOFF# — BKOFF# <36>
RF_OFF#/GPXIOA09 — WL_OFF# <44>
GPXIOA10 — EC_ID
GPXIOA11 — POWER_KEY <35>

PCH_PLT_RST# — R456 100K_0402_5%
R458 2D@ 100K_0402_5% — +3VSB
R459 3D@ 100K_0402_5%

GPI
PM_SLP_S4#/GPXIOD01 — PM_SLP_S4# <13>
ENBKL/GPXIOD02 — ENBKL — R461 0_0402_5% — S_BKOFF <34,35,36>
EAPD/GPXIOD03 — EAPD_CODEC <41>
EC_THERM#/GPXIOD04 — HDMI_CABLE_DET — HDMI_CABLE_DET <38>
SUSP#/GPXIOD05 — SUSP# — SUSP# <24,49,53,54,56,59>
PBTN_OUT#/GPXIOD06 — PBTN_OUT# — PBTN_OUT# <13>
EC_PME#/GPXIOD07 — 3SV_PG — 3SV_PG <52>

V18R — C663 4.7U_0603_6.3V6K

XCLK1 — CRY2 — C662 15P_0402_50V8J
XCLK0 — CRY1 — C664 15P_0402_50V8J
32.768KHZ_12.5PF_Q13MC14610002 Y6 — @ R463 20M_0402_5%
R467 0_0402_5% @ — <13> PCH_SUSCLK

100P_0402_50V8J C876 ON/OFF

+3VSB — @ R465 10K_0402_5% — C665 0.1U_0402_10V6K — R471 0_0402_5% @
+3VSB — U39 @ SN74AHCT1G125GW_SOT353-5 — EC_RSMRST#

+V_3.3V — R550 4.7K_0402_5% — R551 4.7K_0402_5%
EC_SMB_CK2_M — Q61A DMN66D0LDW-7_SOT363-6 — EC_SMB_CK2 — EC_SMB_CK2 <13,21,42>
EC_SMB_DA2_M — Q61B DMN66D0LDW-7_SOT363-6 — EC_SMB_DA2 — EC_SMB_DA2 <13,21,42>

11/4 Change PN of Q61 from SB00000AR00 to SB00000DH00

+3VSB

VOL_SDA_1	4.7K_0402_5%	R967	
VOL_SCL_1	4.7K_0402_5%	R966	
EC_OSD_RST#	2.2K_0402_5%	R947	
BT_RESET	4.7K_0402_5%	R941	
AV_AUDIO_SEL#	4.7K_0402_5%	@ R936	
HDMI_CABLE_DET	4.7K_0402_5%	@ R887	
EC_OSD_CK	4.7K_0402_5%	R854	
EC_OSD_DA	4.7K_0402_5%	R853	
HDMI_SW_EC	10K_0402_5%	R852	
PANEL_STATE_OFF	4.7K_0402_5%	@ R497	
AMP_POWER_DOWN#	4.7K_0402_5%	@ R496	
EC_ESB_INT	2.2K_0402_5%	R771	
GLAN_PCIE_WAKE#	100K_0402_5%	R462	
ON/OFF	4.7K_0402_5%	R464	
POWER_KEY	4.7K_0402_5%	@ R713	
PWR_ON_LED#	8.2K_0402_5%	@ R466	
VOL_SCL	4.7K_0402_5%	R468	
VOL_SDA	4.7K_0402_5%	@ R469	
WL_BLUE_LED#	8.2K_0402_5%	@ R470	
EC_MUTE#	4.7K_0402_5%	R472	

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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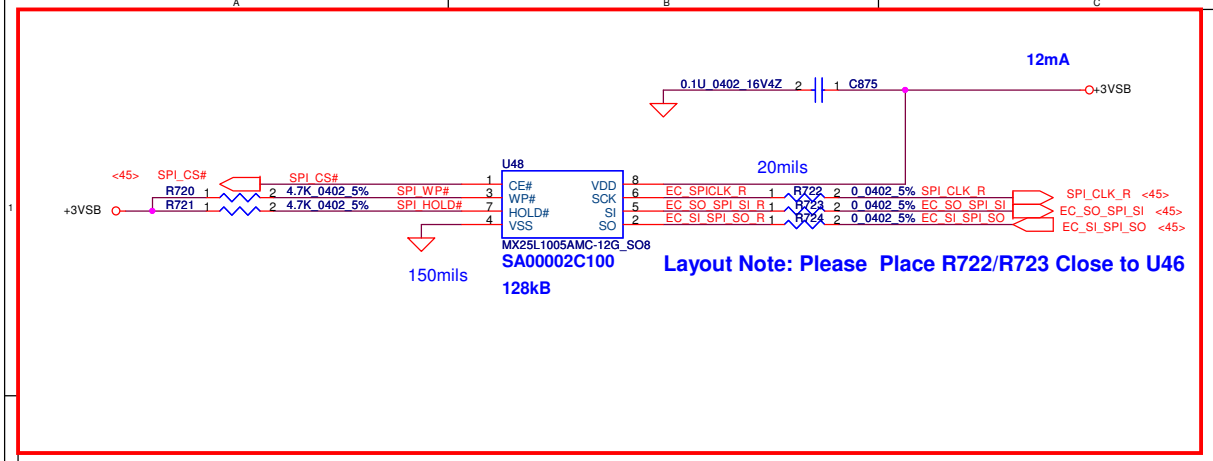
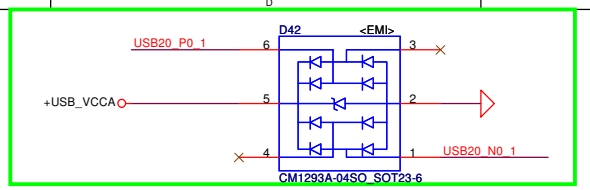
Compal Electronics, Inc.

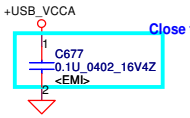
Title: EC KB930/KB conn

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 1.3

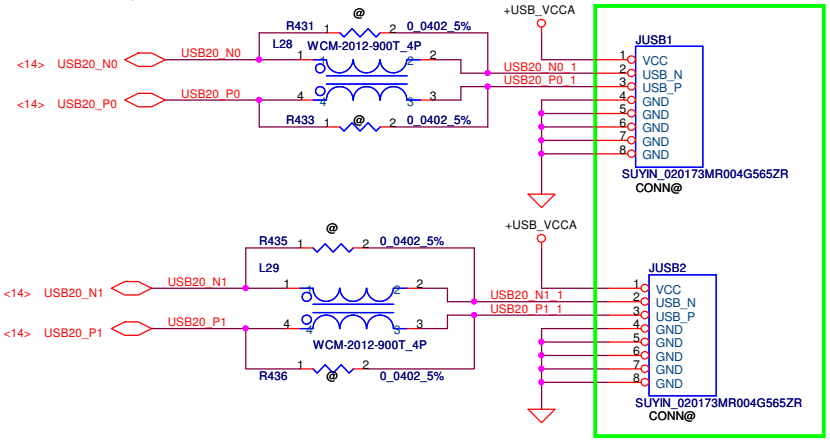
Date: Friday, November 05, 2010 | Sheet 45 of 62





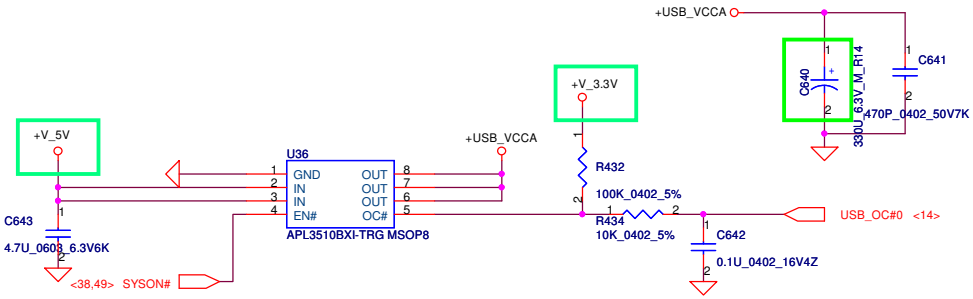


10/25 Change symbol and footprint of D42 from SC300000100 to SC300000O00(ESD request)

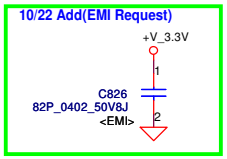


USB Conn. (SIDE)

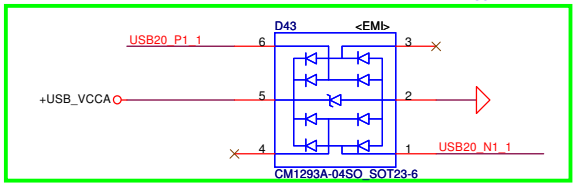
11/2 Change PN of C640 from SF000002Y00 to SF000001G00

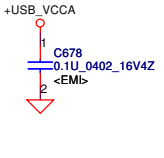


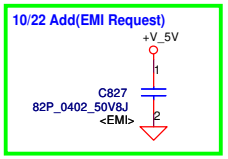
10/22 Add(EMI Request)



8/13 Add D43/C678(EMI Suggest)

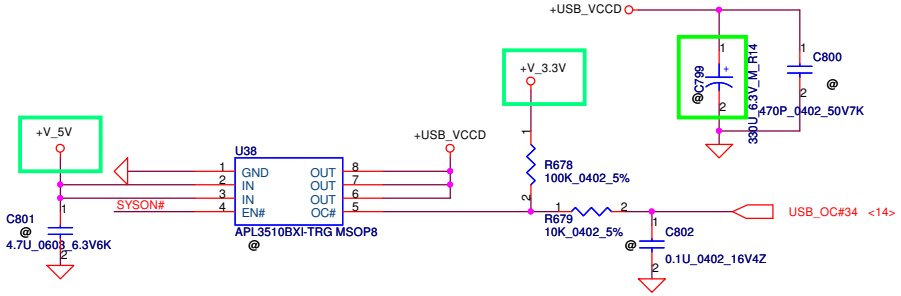




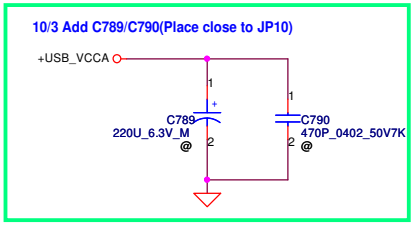


10/25 Change symbol and footprint of D43 from SC300000100 to SC300000O00(ESD request)

11/2 Change PN of C799 from SF000002Y00 to SF000001G00



10/3 Add C789/C790(Place close to JP10)



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Compal Electronics, Inc.

Title: USB / BIOS ROM

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

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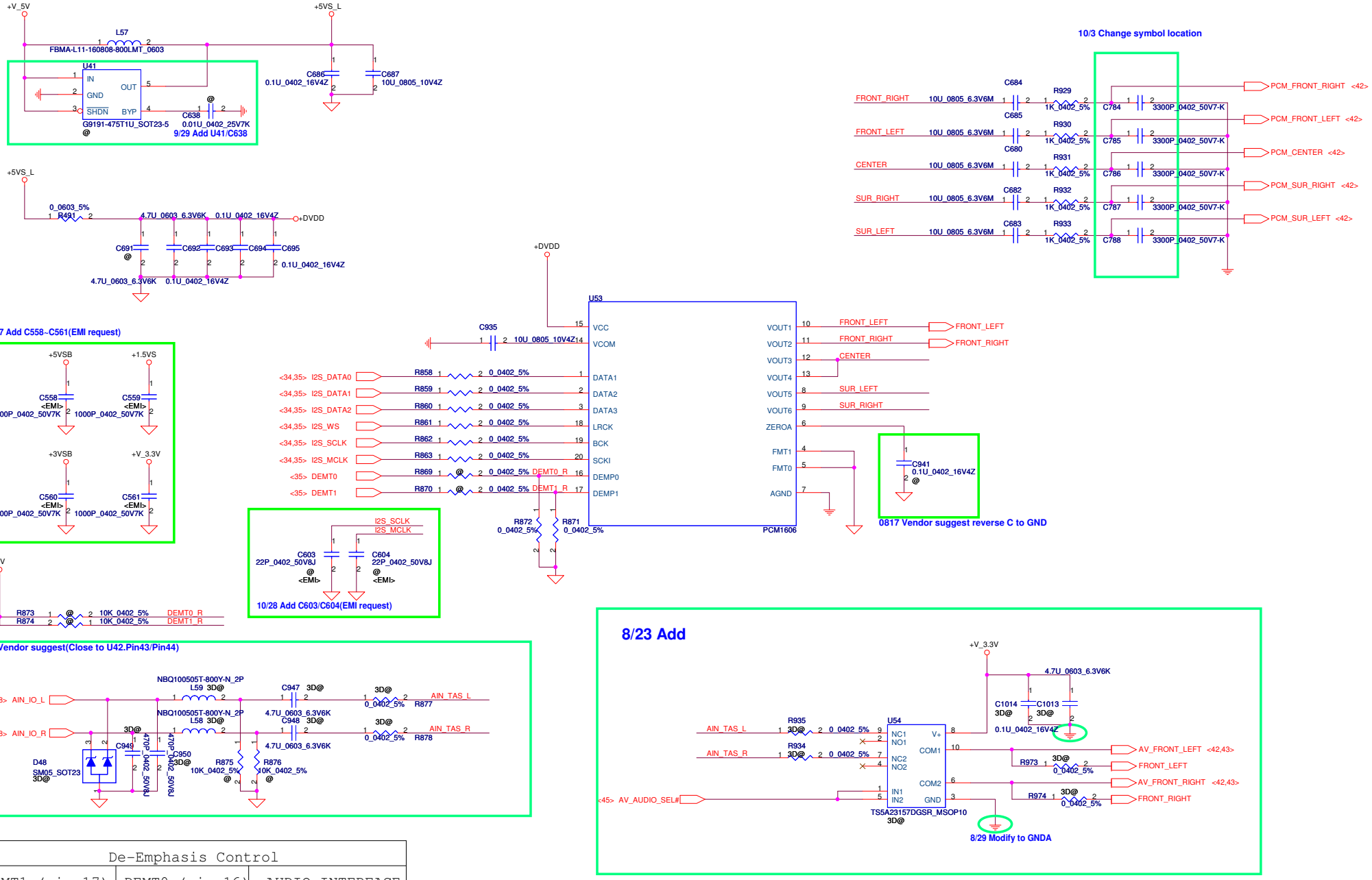

De-Emphasis Control		
DEMT1 (pin 17)	DEMT0 (pin 16)	AUDIO INTERFACE
LOW	LOW	OFF *
LOW	HIGH	48 kHz
HIGH	LOW	44.1 kHz
HIGH	HIGH	32 kHz

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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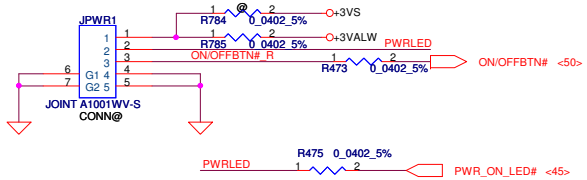
Compal Electronics, Inc.

Title: 5CH AUDIO_PCM1606

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 2.3

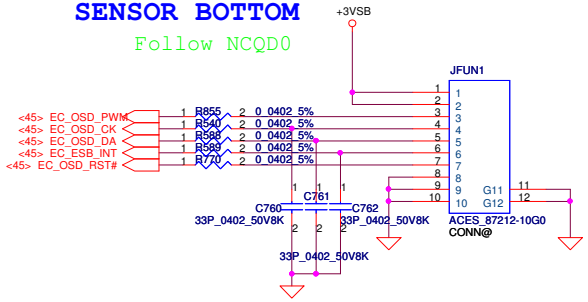
Date: Friday, November 05, 2010 | Sheet 47 of 62

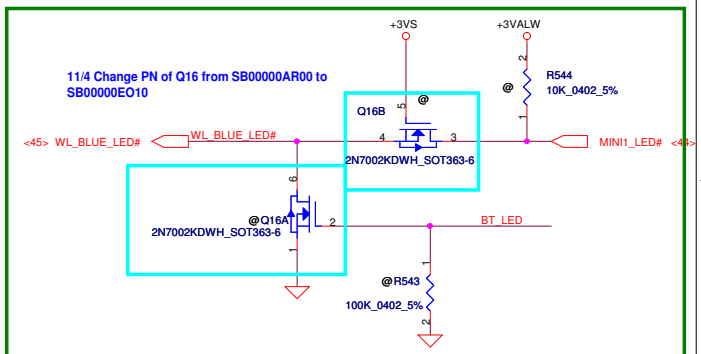
Power switch board



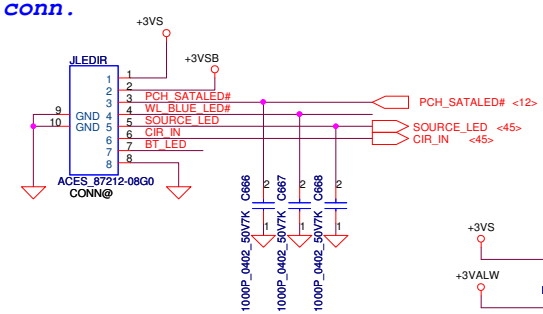
SENSOR BOTTOM

Follow NCQD0

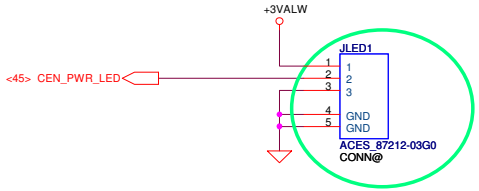




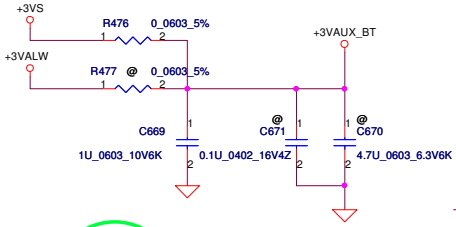
LED board conn.



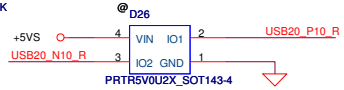
DECO LED board conn.

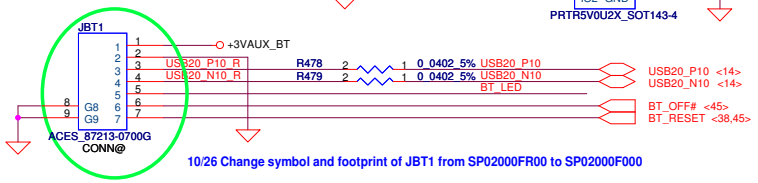


10/3 Change symbol of JLED1 from SP020008V00 to SP02000PO00(4pin to 3pin)



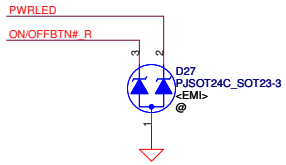
BT Connector

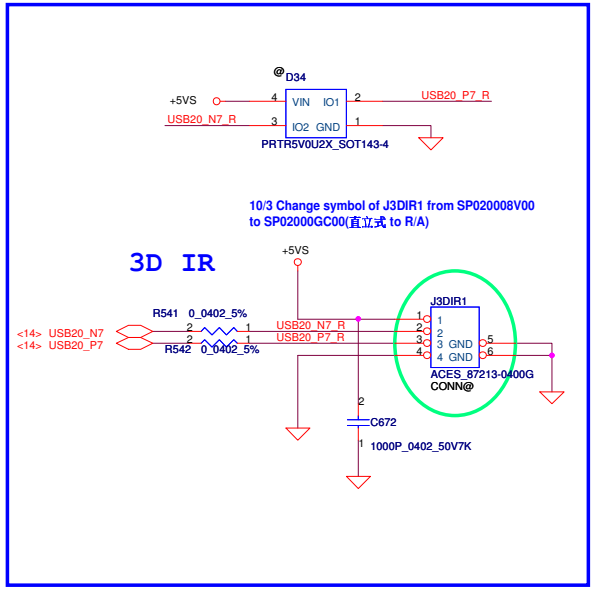




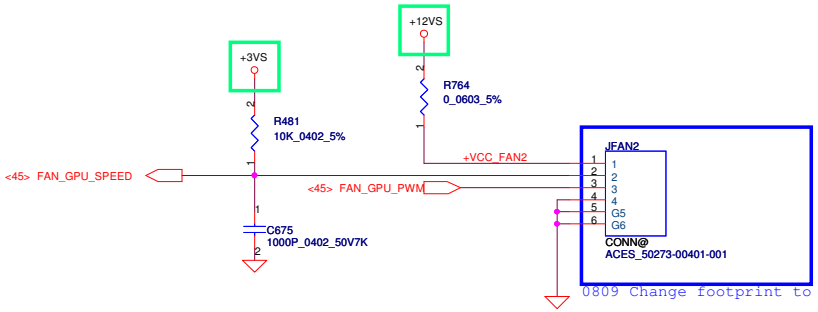
10/26 Change symbol and footprint of JBT1 from SP02000FR00 to SP02000F000

8/13 Change symbol of D27 to SCA00000E00(EMI Suggest)

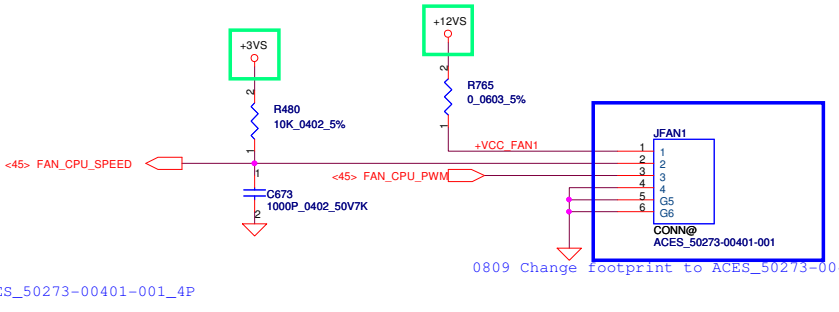




Fan Control circuit



0809 Change footprint to ACES_50273-00401-001_4P



0809 Change footprint to ACES_50273-00401-001_4P

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Compal Electronics, Inc.

Title: WL/BT ON/OFF, PWR S/W, OSD

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.3

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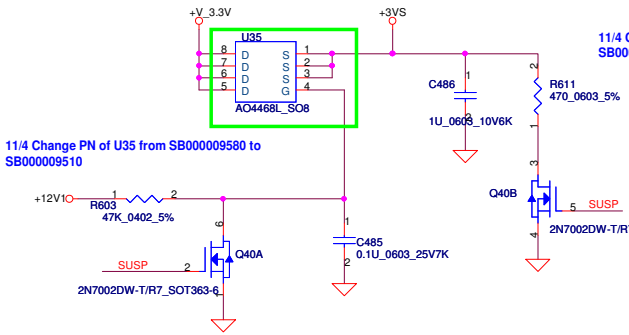
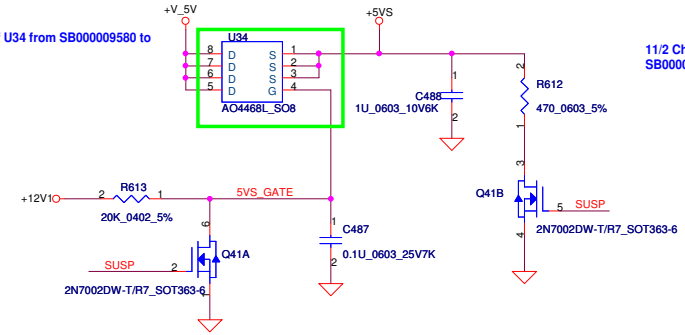
+V_3.3V TO +3VS



11/4 Change PN of U35 from SB000009580 to SB000009510

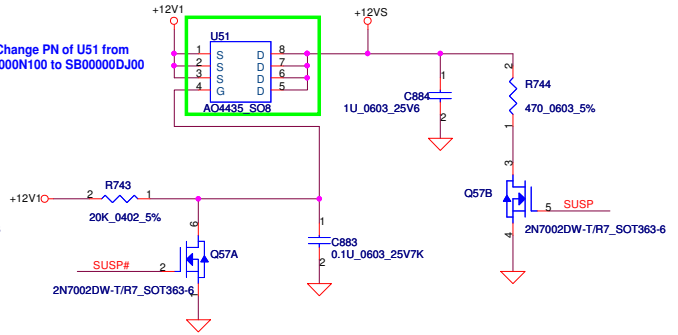
11/4 Change PN of U34 from SB000009580 to SB000009510

+V_5V TO +5VS

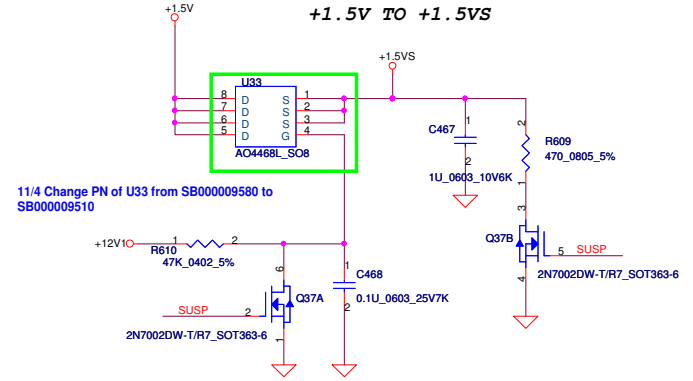


11/2 Change PN of U51 from SB00000N100 to SB00000DJ00

+12V1 TO +12VS

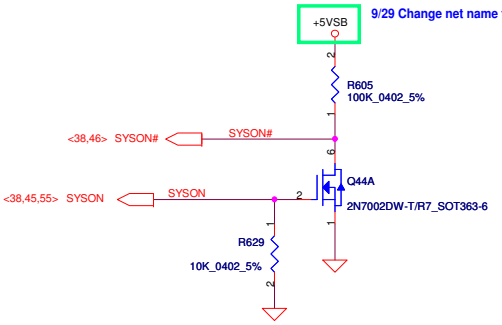


+1.5V TO +1.5VS

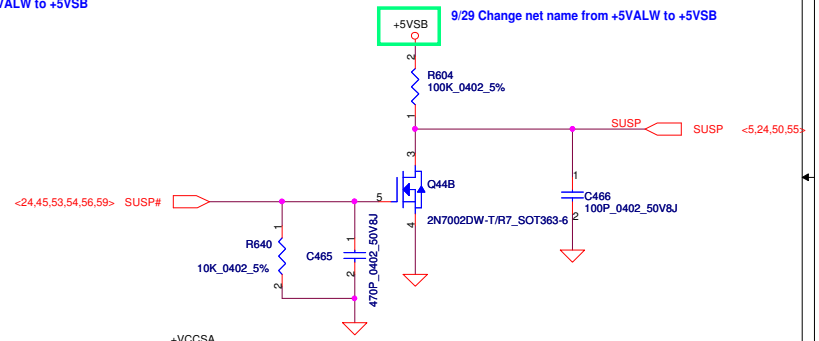


11/4 Change PN of U33 from SB000009580 to SB000009510

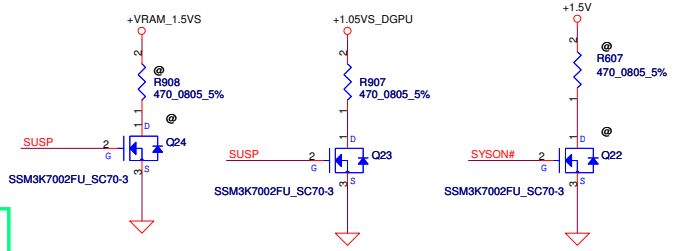
9/29 Change net name from +5VALW to +5VSB

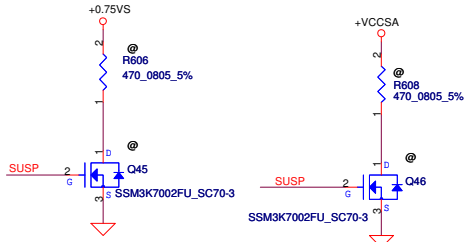


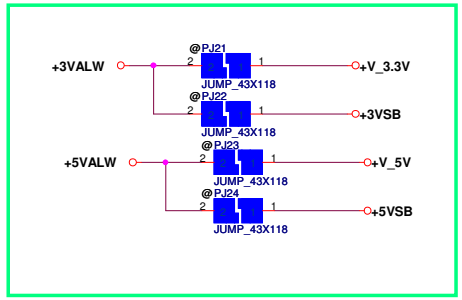
9/29 Change net name from +5VALW to +5VSB



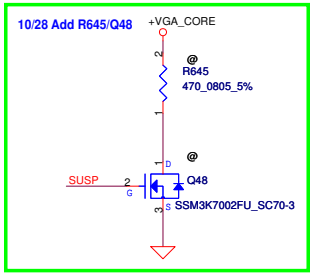
Discharge circuit



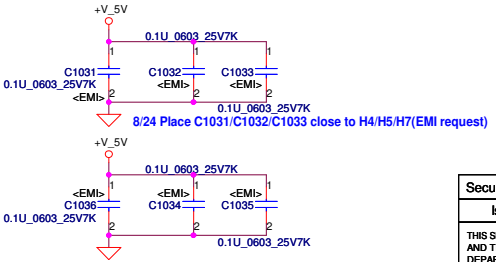




10/28 Add R645/Q48



8/24 Add C1031~C1036

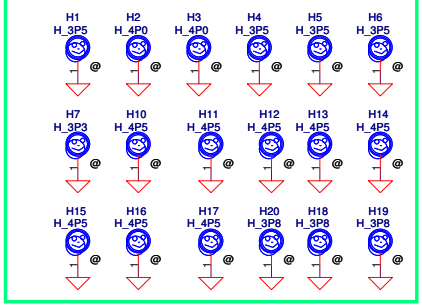


8/24 Place C1031/C1032/C1033 close to H4/H5/H7(EMI request)

8/24 Place C1034/C1035/C1036 close to H1/H2/H6(EMI request)

NON-PDH

Screw



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Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Compal Electronics, Inc.

Title: DC Interface/Screw

Size: B | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

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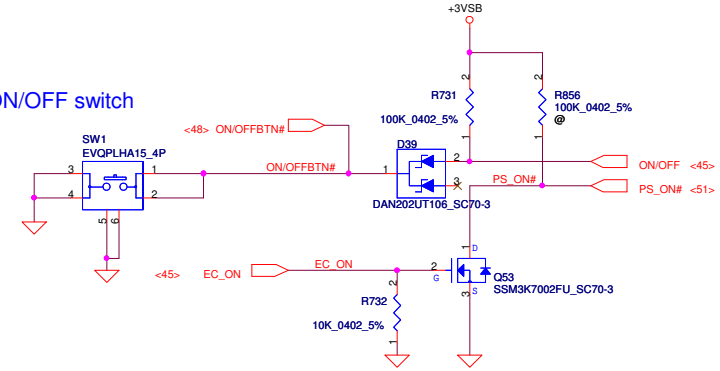
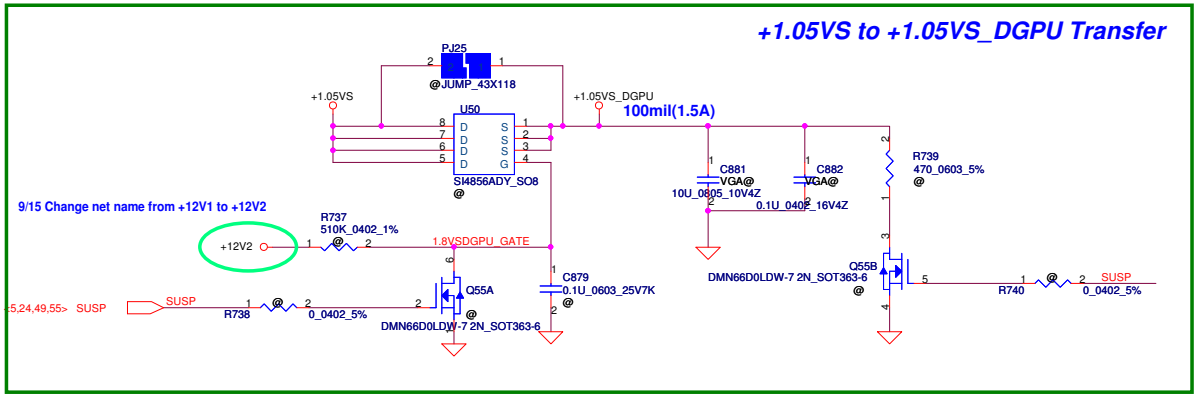
Power Button

ON/OFF switch



+1.05VS to +1.05VS_DGPU Transfer



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Compal Electronics, Inc.

Title: Power OK/PBN

Size: B | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

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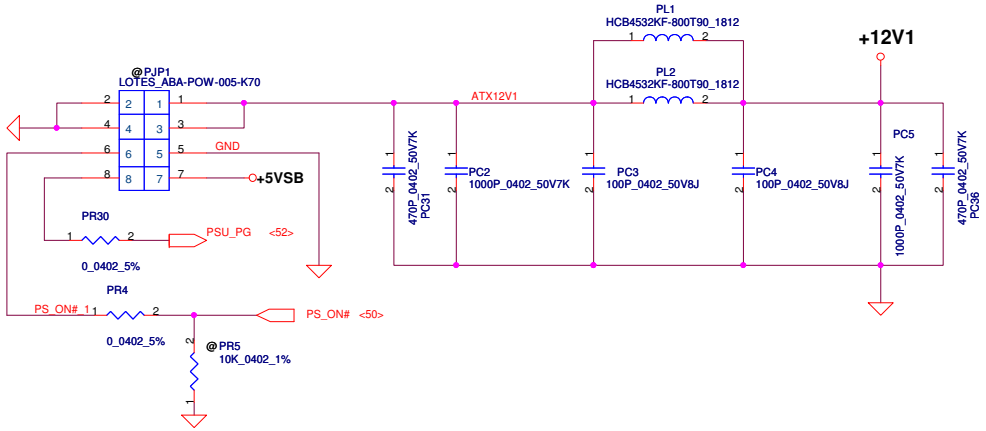
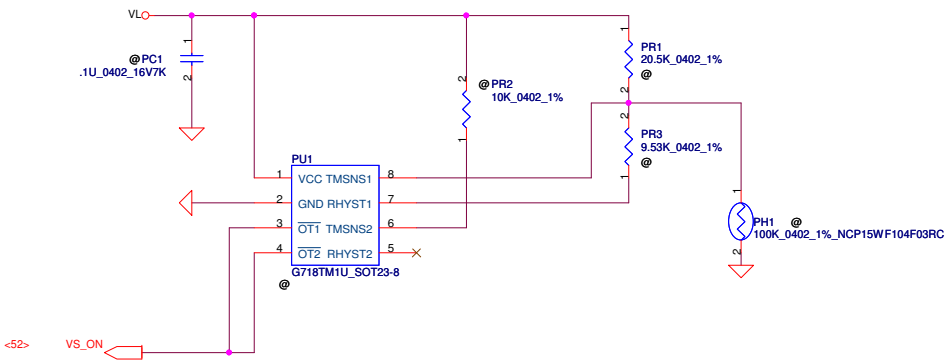
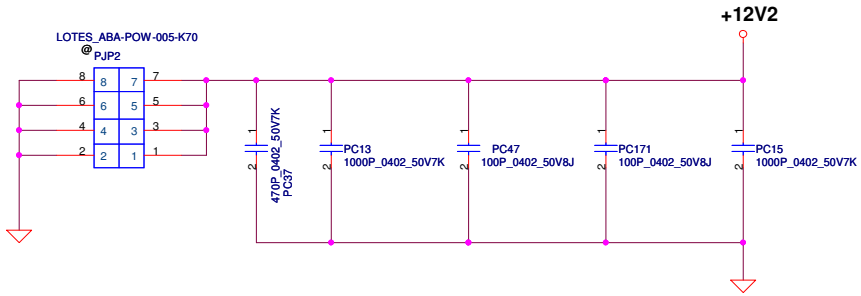
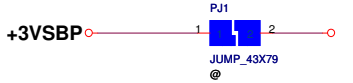
PH1 under CPU botten side :

CPU thermal protection at 92 degree C
Recovery at 57 degree C

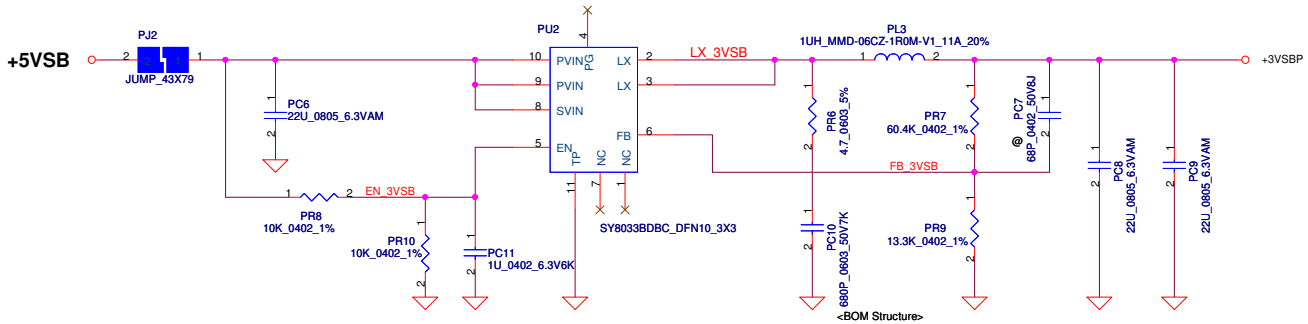








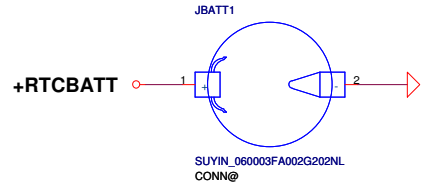
FOR EC suspend



VFB=0.6V
Vo=VFB*(1+PR7/PR9)=3.318 V

Ipeak=0.062A, Imax=0.045A

Current limit >4A



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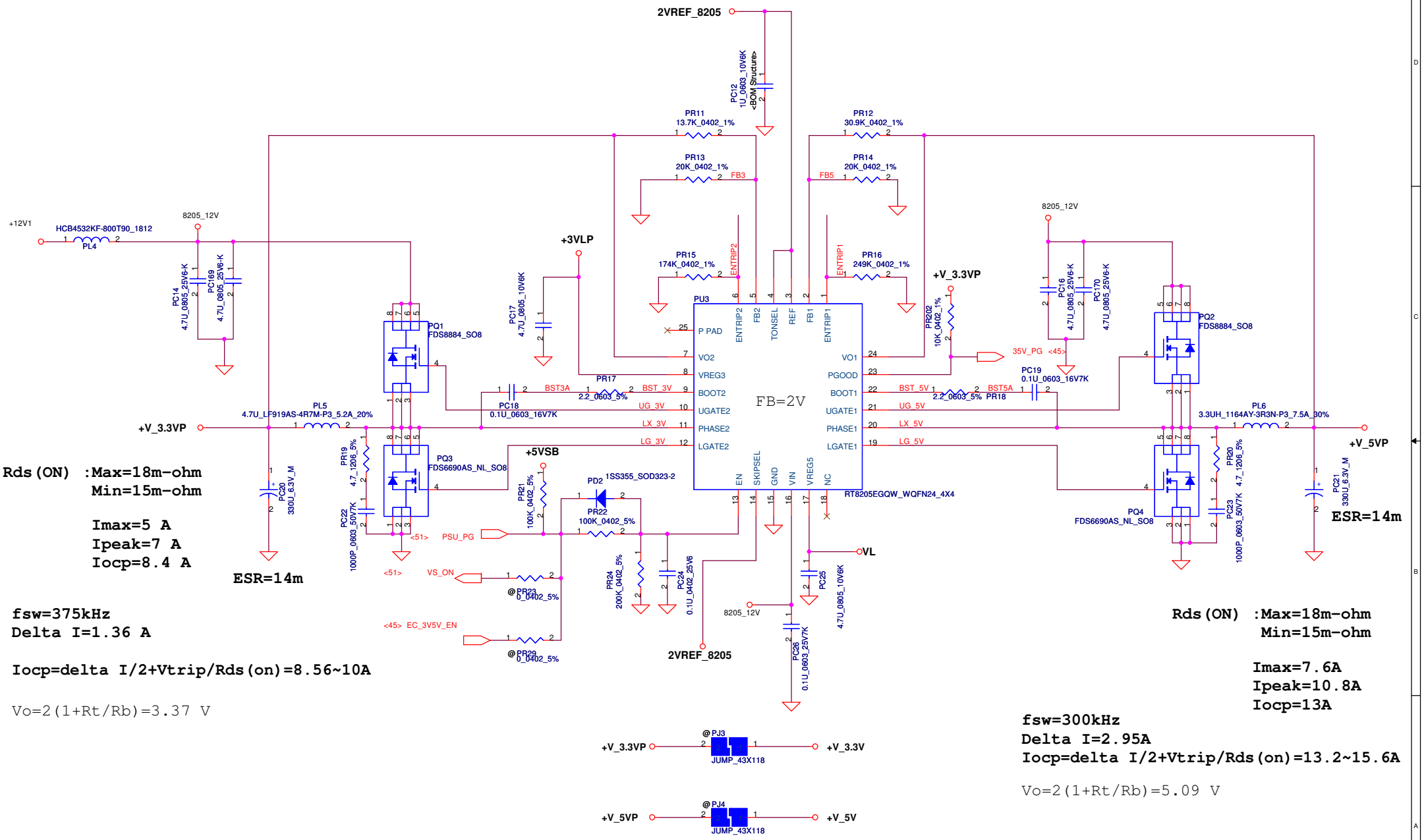
Date: Friday, November 05, 2010		Sheet 51 of 62	



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Issued Date	2010/07/20	Deciphered Date	2011/07/20

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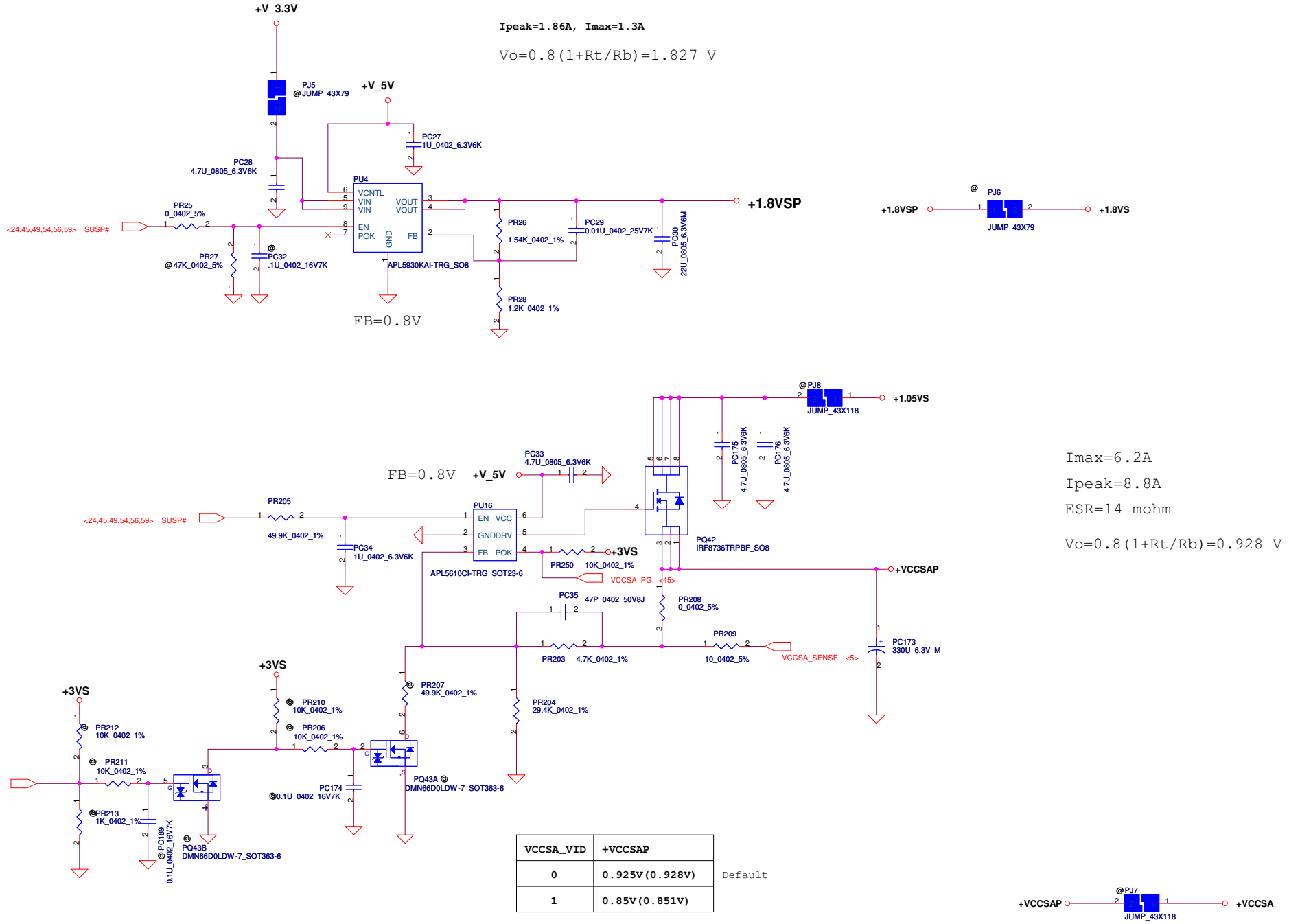
Compal Electronics, Inc.

Title: +V_5VP/ +V_3VP

Size: Custom | Document Number: 0.3 | Rev:

Date: Friday, November 05, 2010 | Sheet 52 of 62



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Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Compal Electronics, Inc.

Title: +VCCSA/+1.8VSP

Size	Document Number	Rev
Custom		0.3

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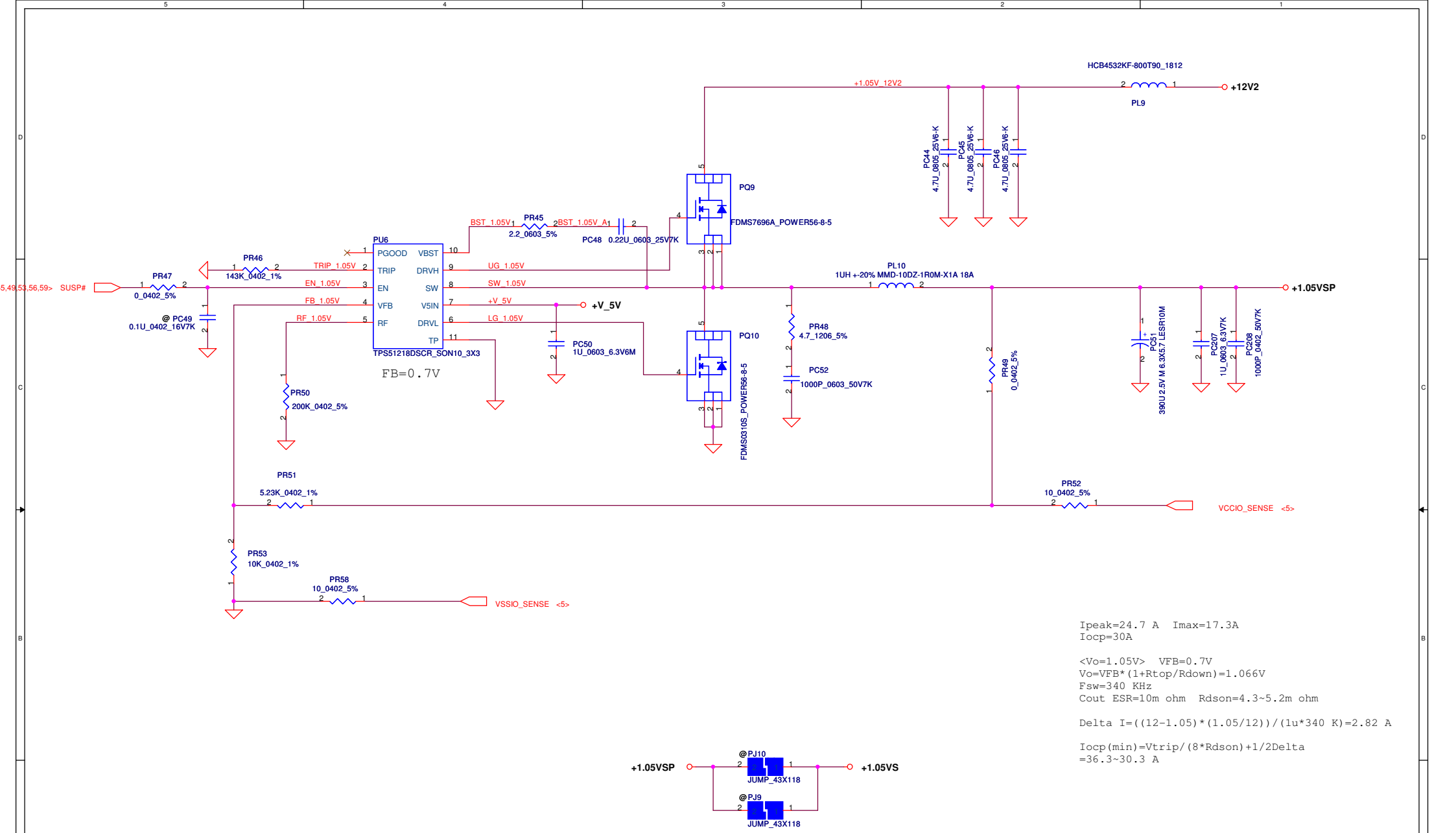

Ipeak=24.7 A Imax=17.3A
Iocp=30A

<Vo=1.05V> VFB=0.7V
Vo=VFB*(1+Rtop/Rdown)=1.066V
Fsw=340 KHz
Cout ESR=10m ohm Rdson=4.3~5.2m ohm

Delta I=((12-1.05)*(1.05/12))/(1u*340 K)=2.82 A

Iocp(min)=Vtrip/(8*Rdson)+1/2Delta
=36.3~30.3 A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/07/20	Deciphered Date	2011/07/20
Title	+1.05VSP		
Size: Custom	Document Number		Rev: 0.3
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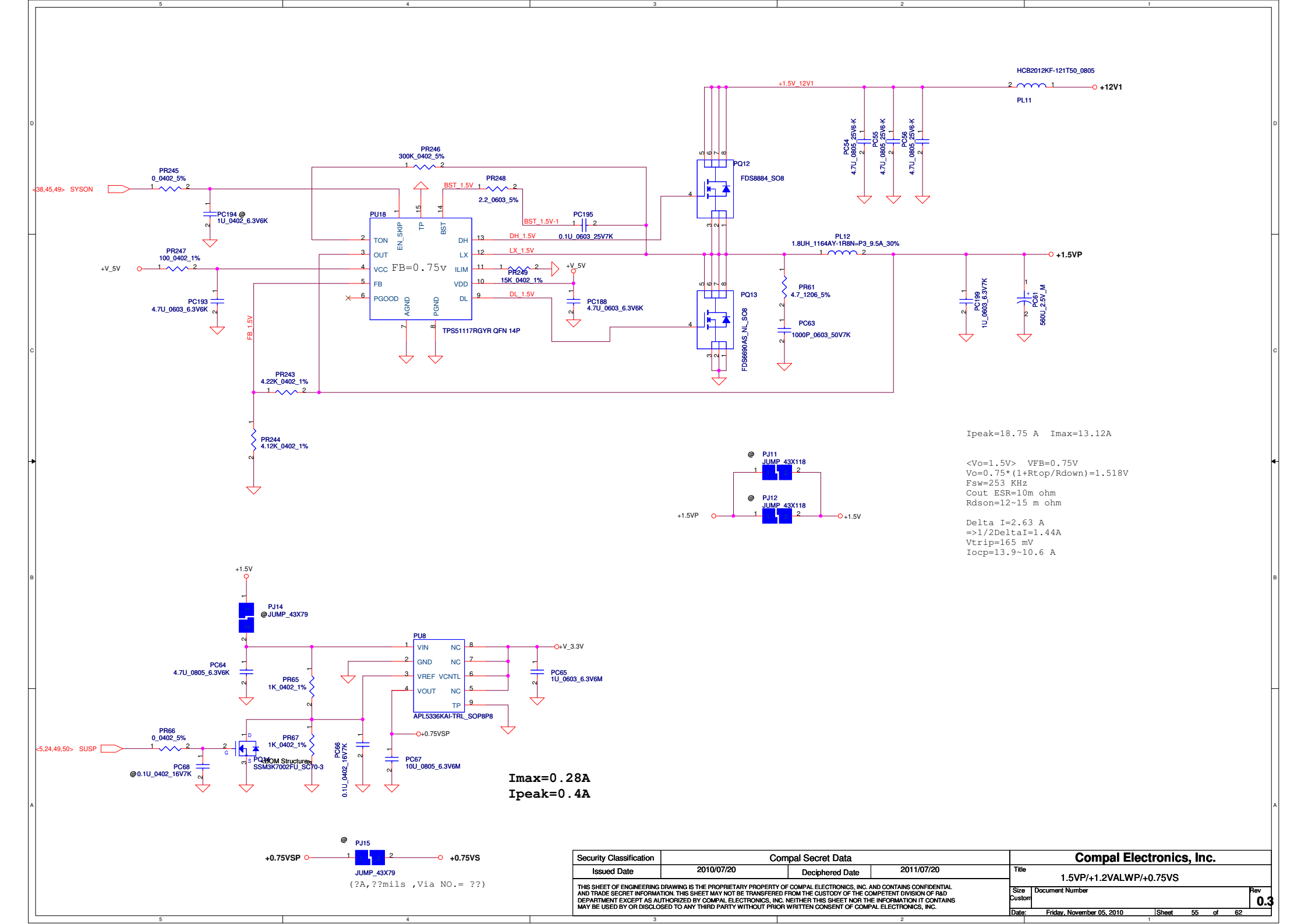

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Compal Electronics, Inc.

Title	1.5VP/+1.2VALWP/+0.75VS	
Size: Custom	Document Number	Rev: 0.3
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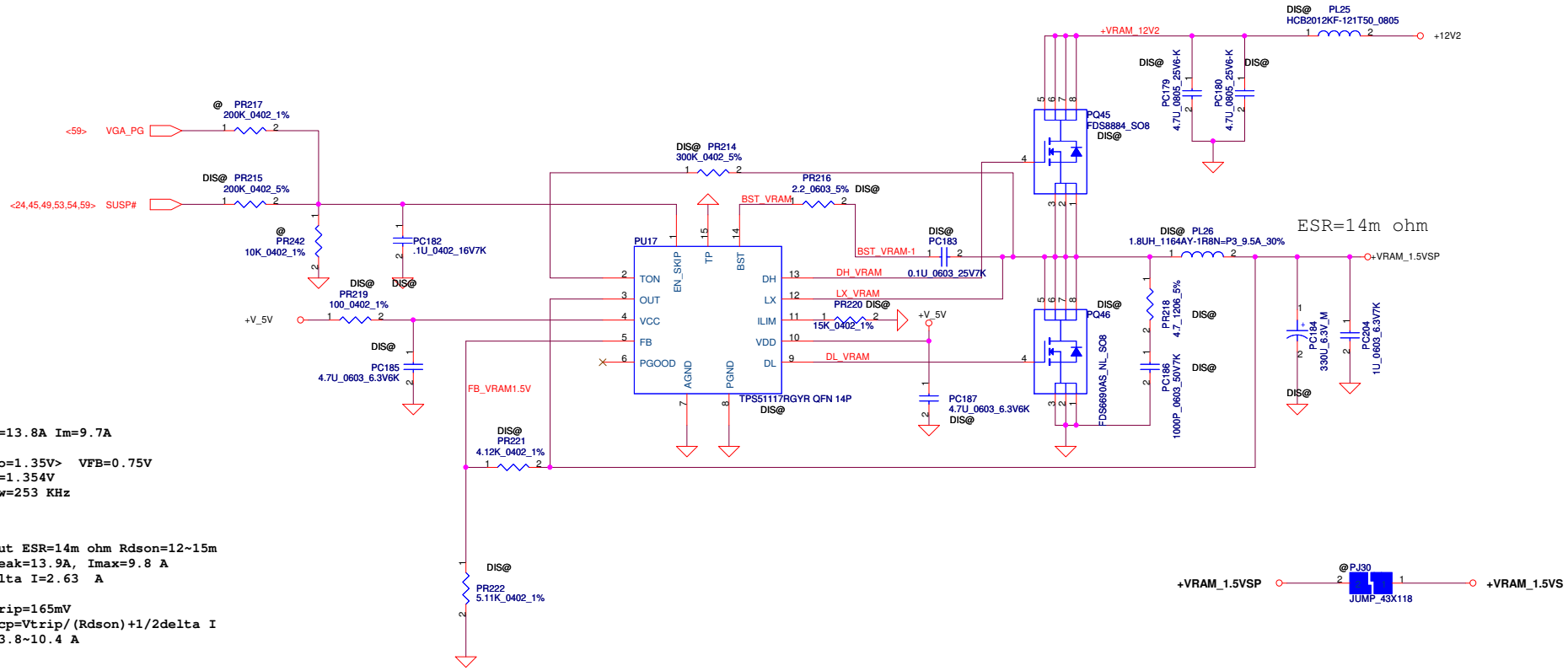

Ip=13.8A Im=9.7A

<Vo=1.35V> VFB=0.75V
Vo=1.354V
Fsw=253 KHz

Cout ESR=14m ohm Rdson=12~15m
Ipeak=13.9A, Imax=9.8 A
Delta I=2.63 A

Vtrip=165mV
Iocp=Vtrip/(Rdson)+1/2delta I
=13.8~10.4 A

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Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Compal Electronics, Inc.

Title: VCCPP/1.8VP

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

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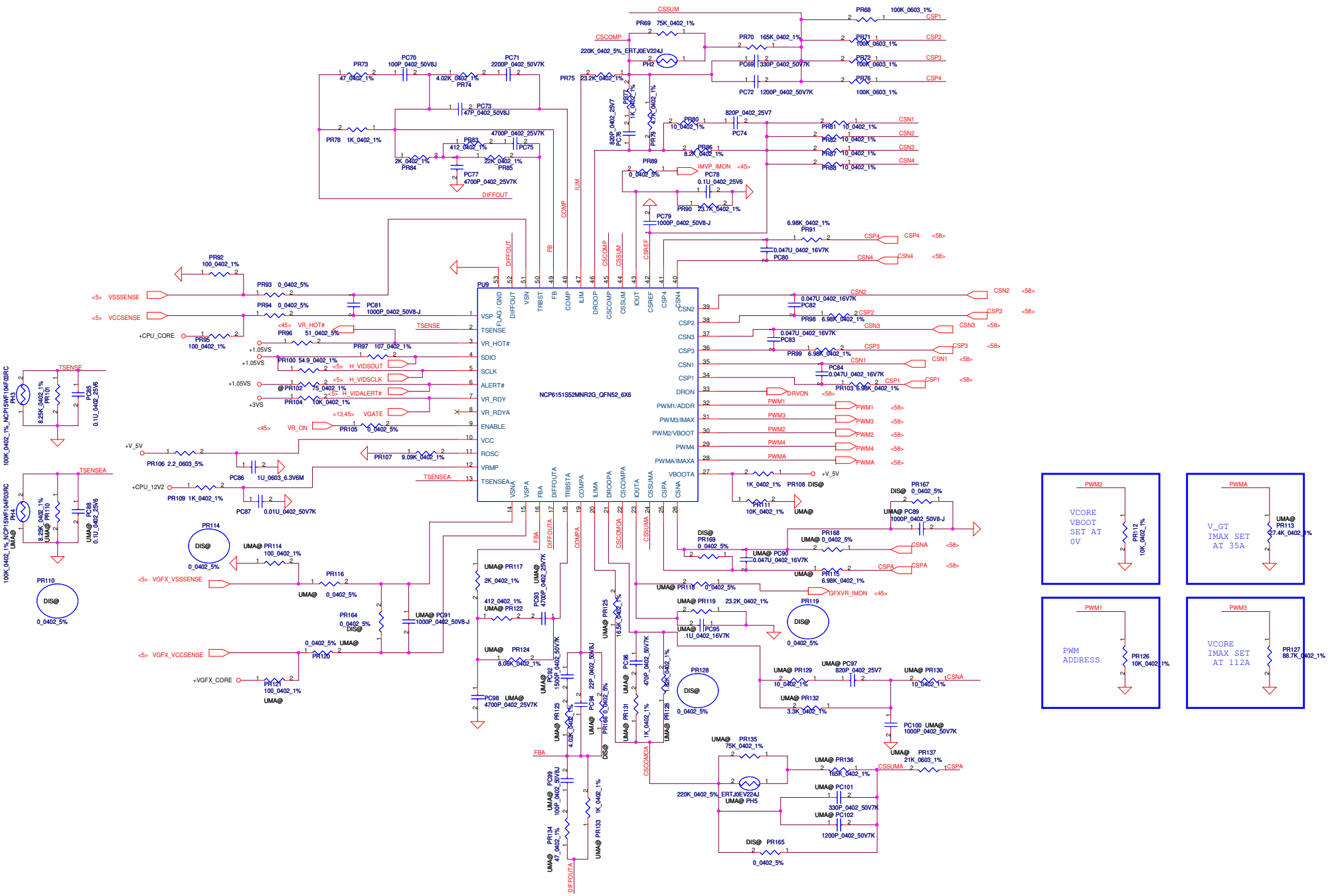

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Compal Electronics, Inc.

Title: CPU_CORE_1

Size	Document Number	Rev
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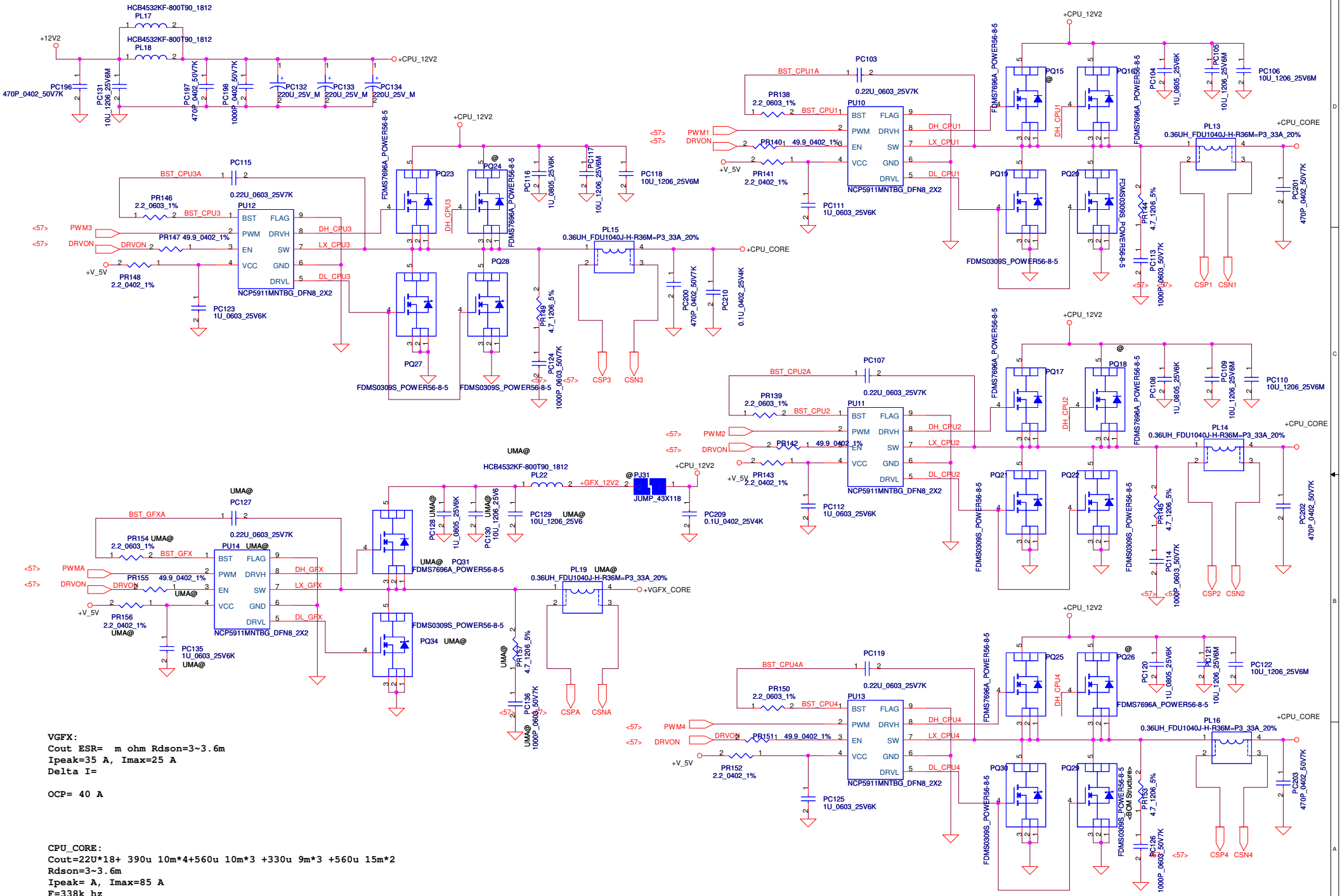

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Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Compal Electronics, Inc.

Title: CPU_CORE_2

Size	Document Number	Rev
Custom		0.3

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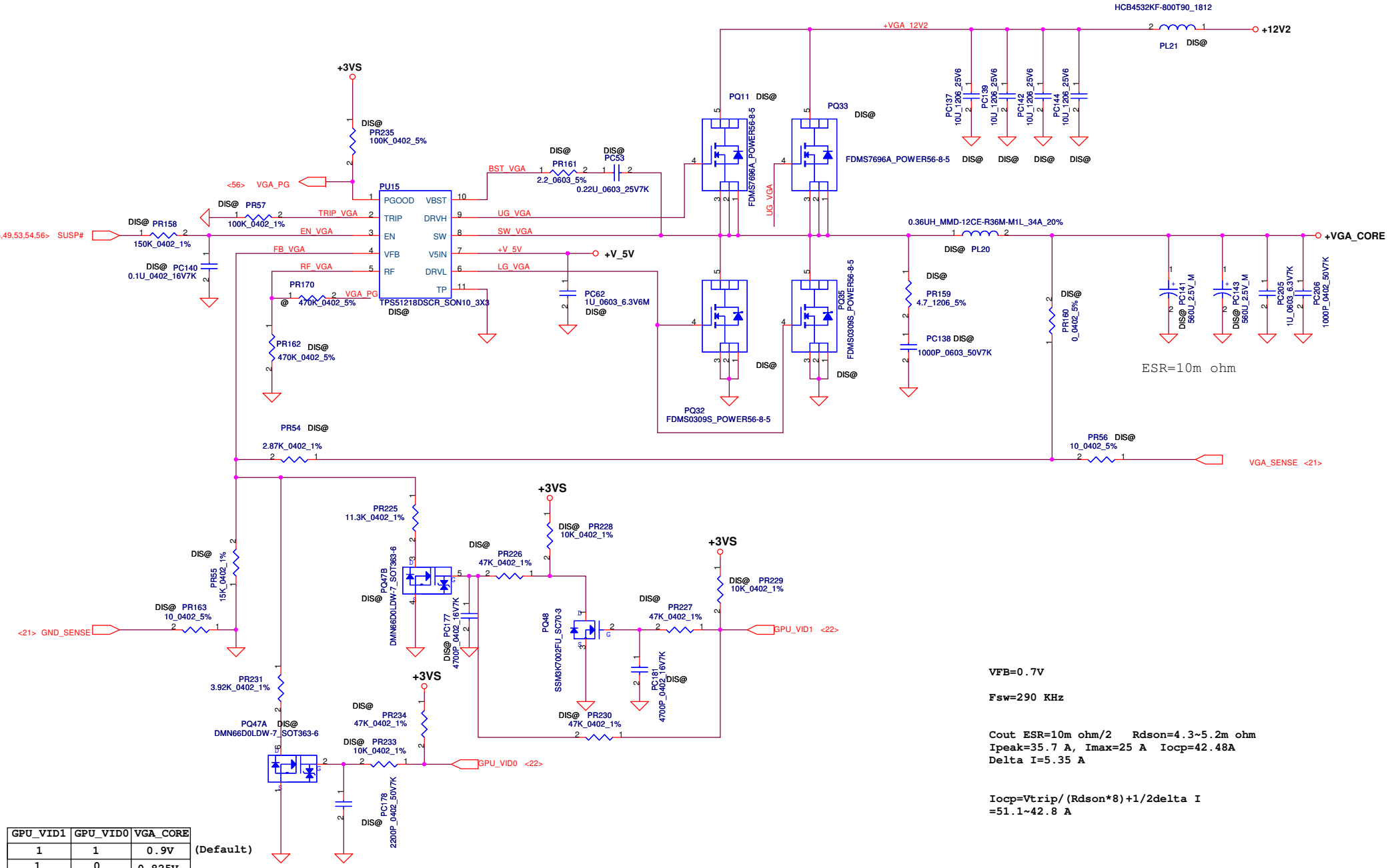

VFB=0.7V

Fsw=290 KHz

Cout ESR=10m ohm/2 Rdson=4.3~5.2m ohm
Ipeak=35.7 A, Imax=25 A Iocp=42.48A
Delta I=5.35 A

Iocp=Vtrip/(Rdson*8)+1/2delta I
=51.1~42.8 A

GPU_VID1	GPU_VID0	VGA_CORE	
1	1	0.9V	(Default)
1	0	0.825V	
0	1	1.075V	

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Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Compal Electronics, Inc.

Title: VGA_CORE

Size: Custom | Document Number | Rev: 0.3

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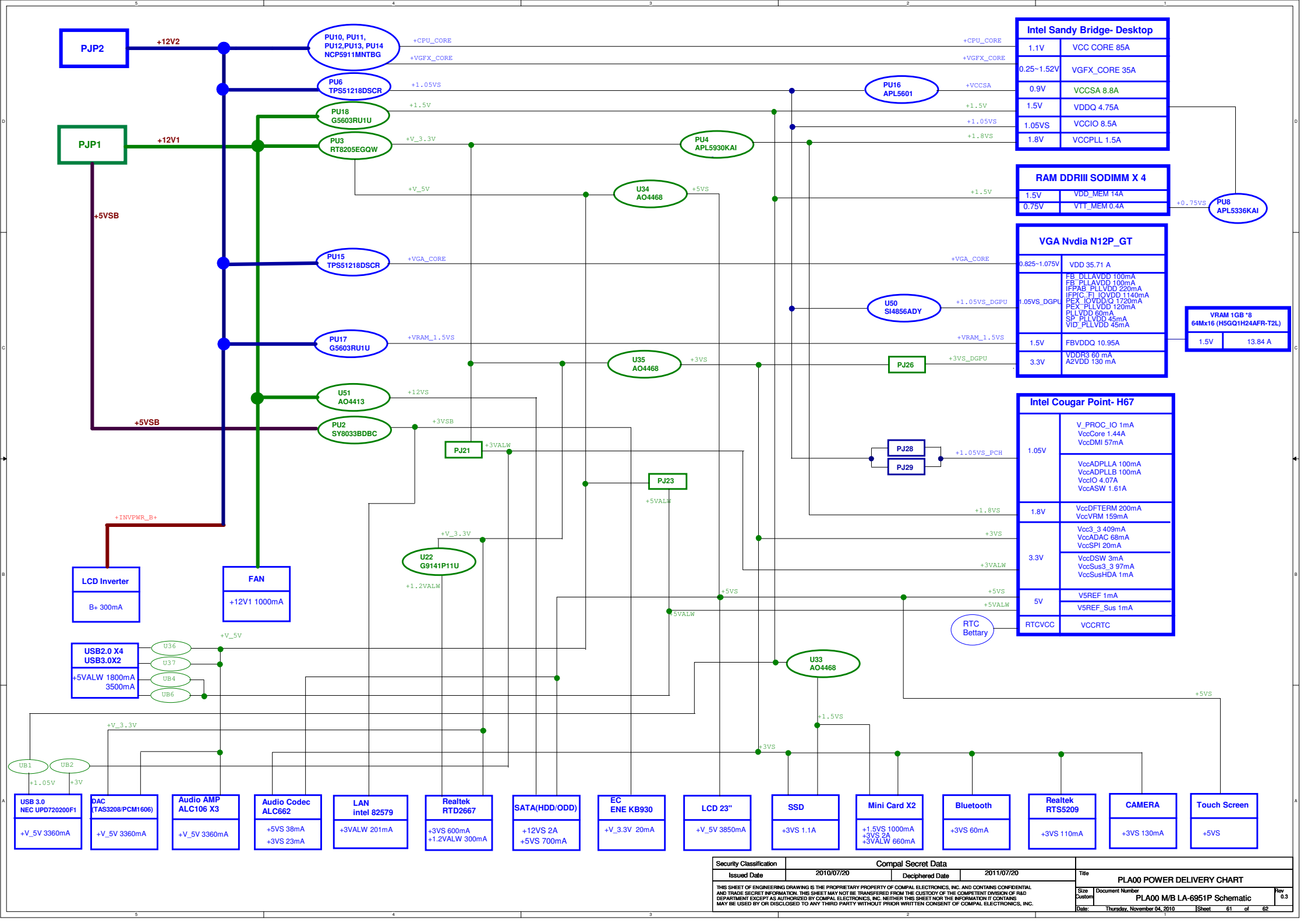
Title	<Title>	
Size: A	Document Number: PLA00 M/B LA-6951P Schematic	Rev: 0.3
Date: Thursday, November 04, 2010	Sheet 60 of 62	



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Title: PLA00 POWER DELIVERY CHART

Size	Document Number	Rev
Custom	PLA00 M/B LA-6951P Schematic	0.3

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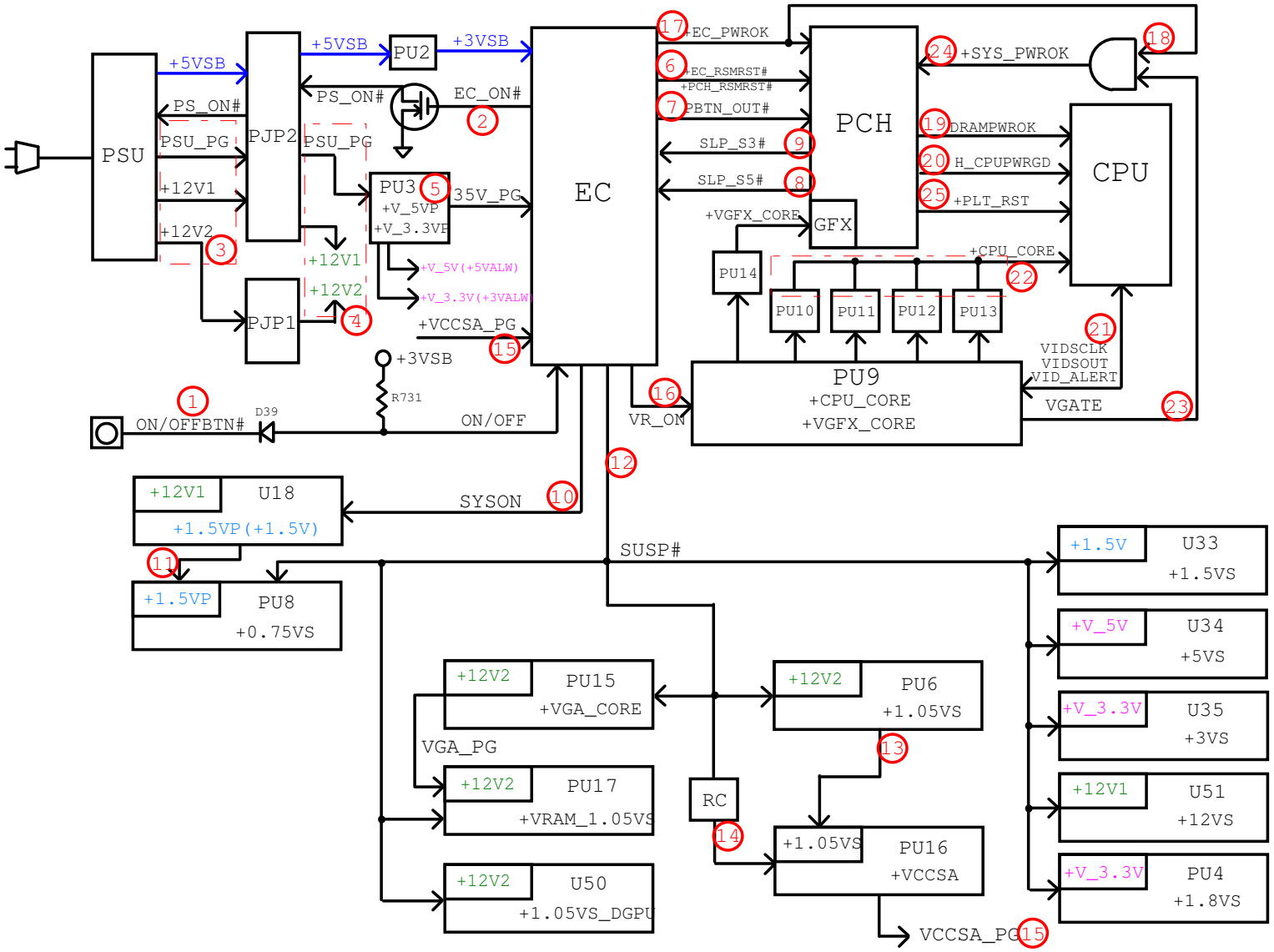
COMPAL CONFIDENTIAL

MODEL NAME: *PLA00 Power Sequence Block Diagram (Discrete)*
PCB NAME: *LA6951P*
REVISION: *0.3*
DATE: *2010/10/26*



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Title: Power Sequence Block Diagram

Size: Custom | Document Number: PLA00 M/B LA-6951P Schematic | Rev: 0.3

Date: Thursday, November 04, 2010 | Sheet 62 of 62

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